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Si, SiGe Nanowire Devices by Top–Down Technology and Their Applications

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Invited Paper

***Abstract*—Nanowire (NW) devices, particularly the gate-all-around (GAA) CMOS architecture, have emerged as the front-runner for pushing CMOS scaling beyond the roadmap. These devices offer unique advantages over their planar counterparts which make them feasible as an option for 22-nm and beyond technology nodes. This paper reviews the current technology status for realizing the GAA NW device structures and their applications in logic circuit and nonvolatile memories. We also take a glimpse into applications of NWs in the "more-than-Moore" regime and briefly discuss the application of NWs as biochemical sensors. Finally, we summarize the status and outline the challenges and opportunities of the NW technology.**

***Index Terms*—Gate-all-around (GAA) nanowire (NW) transistors, Nonvolatile memory (NVM), NW CMOS, NW logic, top–down technology.**

I. Introduction

FEATURE-SIZE scaling in CMOS technology has continued to follow the diktat of Moore's law [1] for more than 40 years. Although the structure remained planar, the CMOS device architecture has undergone many a mutation to sustain the scaling pace. Implementation of LDD, lateral nonuniformity in channel doping, reduction in junction depth, and vertical nonuniformity in well doping including pocket and HALO implants are a few examples. In addition, the performance of scaled devices has been further improved by introducing stressors in the structure to improve mobility [2], [3]. The gate leakage current issue is tackled by the following ways: 1) slowing down the scaling of the gate oxide thickness and 2) introducing high-k materials in the gate dielectric [4]. Circuits of 45 nm with high-k and metal gates are in production [5].

The device scaling, however, appears to be reaching the end-of-the-technology roadmap [6]. The major challenges being faced in further scaling are as follows: 1) degraded gate electrostatic control of the channel potential leading to short-channel effects—threshold voltage roll-off, large DIBL, and poor subthreshold slope (SS); 2) increased gate and junction leakages; 3) reduced channel mobility; and 4) increased source/drain (S/D) resistance. The increased doping in the channel which is needed to help the control of the gate over the channel vis-à-vis that of source and drain terminals leads to degraded performance.

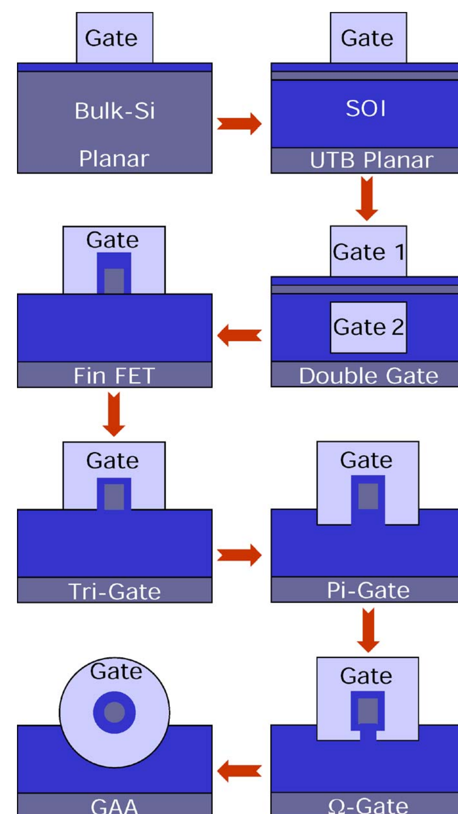

Fig. 1. Progression of device structure from single-gated planar to fully GAA NW MOSFETs.

The electrostatics gets improved in multiple-gate structures [7] as the gate influences the channel potential from more than one side and thus relaxes the demand on the doping. Fig. 1 shows the evolution of multiple-gate transistors schematically in the order of increasing gate electrostatic control. Apparently, the gate-all-around (GAA) structure is the most resistant to short-channel effects among all the emerging device structures for a given silicon body thickness. The simulations [8] indicate

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that in cylindrical GAA architecture, the gate length can be scaled to 5 nm with the corresponding scaling of the intrinsic nanowire (NW) channel body. Furthermore, the cylindrical geometry gives inverse logarithmic dependence of the gate capacitance on the channel diameter, and thus, the gate length in these devices can be scaled with wire diameter without reducing the gate dielectric thickness. It also makes the GAA NW architecture an excellent candidate for SONOS-type nonvolatile memory (NVM) applications where the gate dielectric has to be necessarily thicker.

Interestingly, the NW structures provide for very large surface-to-volume ratio that makes them ideal structures for sensing of chemical/biochemical species [9]. The NW surface can be sensitized to bind [10] the target species which has a magnified impact on the electrical transport in the body of the NW due to its smaller volume.

The fabrication technology of NW channels can be broadly categorized into two groups, namely, 1) the bottom–up approach and 2) the top–down approach. In the case of bottom–up approach, the wire channels are synthesized, for example, using vapor–liquid–solid chemistry [11], typically with the help of a metal catalyst. Many approaches have been investigated for assembly [12]–[14], including the templated growth [15] of NWs. Fabrication of silicon NWs (Si-NWs) and devices has also been reported using etching, with the platinum NW masks being prepared with the help of the superlattice NW pattern transfer (SNAP) process [16], [17]. NWs have also been synthesized in the "microcracks" induced in the thin films using stress for templated growth [18].

The bottom–up approaches involving synthesis of NWs have been extensively reviewed in the literature, for instance, by Xia *et al.* [11], Law *et al.* [19], and Lu and Lieber [20], and are not discussed in further detail in this paper. In the top–down approach, the NWs are prepared in place utilizing lithography and etch processes, followed by trimming or stress-limited oxidation techniques. Integration of top–down-fabricated NWs in circuit functionality is straightforward, while the bottom–up approach faces a daunting challenge of assembling the wires into circuit functions.

This paper reviews the current status of the NW technology and applications, with a particular focus on the top–down approach and the GAA NW CMOS device architecture. The top–down fabrication approaches proposed by different groups are reviewed in Section II. The device electrical characterization and carrier transport results are reviewed in Section III. Recently reported circuit implementations using these novel devices are discussed in Section IV. The application of the GAA NW architecture as NVM is discussed in Section V. Section VI briefly reports the results for different sensor applications of the NW-based devices. The challenges and opportunities of the NW technology are discussed in Section VII, and conclusions are summarized in Section VIII.

II. NW AND GAA NW DEVICE FABRICATION

There are a few variants of fabrication approaches reported for the realization of NWs and devices using the top–down technique. All approaches start with the silicon wafers as the substrate and involve lithography and etching processes for starting pattern definition. Different process steps such as hard-mask trimming [21], etching in H_2 ambient [22], and/or stress-limited oxidation processes [23] follow to convert the silicon structures defined in the earlier step into NWs. The stress-limited oxidation is usually carried out at low temperature to keep the grown oxide in stress to progressively slow down the oxidation rate, thus leaving a nanometer-scale silicon core embedded in the oxide. The stress-limited oxidation was first reported on vertical 1-D nanorod structures by Liu *et al.* [23] wherein the silicon columns of about 40–50 nm in diameter and about 1000 nm in height were subjected to long oxidation (up to more than 40 h) at low temperatures (800 °C) that reduced the core of the silicon to less than 5 nm.

Kedzierski *et al.* [24] made use of this stress-limited oxidation for obtaining the lateral NWs and utilized those as transistor channels, with the thick stress-limited grown oxide serving as the gate dielectric. Although the gate dielectric thickness was large (~25 nm), the devices showed good performance in terms of on-current, on-to-off-current ratios, DIBL, as well as SS.

As an alternative approach for reducing the fins to NWs, hydrogen annealing of an ultranarrow fin has been used by Yang *et al.* [25]. NWs with 10-nm diameter and truncated cylindrical shape have been fabricated. The fabricated sub-10-nm-gate-length NW FETs in omega gate architecture showed very low OFF-state leakage current and excellent gate delay. Hydrogen annealing has also been reported by Ernst *et al.* [26] with vertically stacked NW for high-performance circuits. Tezuka *et al.* [22] have applied hydrogen annealing/etching for Si and SiGe NWs to reduce the sidewall roughness.

Another approach to define Si-NWs and GAA transistors has been reported by Suk *et al.* [21] and Yeo *et al.* [27]. In this approach, silicon fin is split into two NWs—twin Si-NW—using the hard-mask trimming process. The lateral dimensions of NWs are defined by trimming of the hard mask, while the vertical dimensions are given by the thickness of the silicon epitaxial layer on top of a sacrificial SiGe layer. The GAA transistors fabricated on these 8-nm-thick wires with grown oxide as the gate dielectric and damascene poly-silicon gate electrodes down to the physical gate length of 15 nm show excellent gate control and other characteristics.

Our group at IME, Singapore, has extensively implemented the self-limiting oxidation process for Si-NW fabrication in lateral as well as vertical architectures. The wires have been carefully released by etching away the grown oxide in dilute HF [28], [29]. Fig. 2 shows the SEM images of various combinations of NWs fabricated using the lithographic pattern transfer and self-limiting oxidation processes. The different NW shapes and arrangements are a result of variants defined on the mask.

Fig. 2(a) shows a 0.85-μm-long single NW obtained from a low-aspect-ratio fin. Fig. 2(b) shows vertically aligned twin NWs fabricated out of a single high-aspect-ratio fin, with the top-left inset showing the TEM image of a partially oxidized fin and the bottom-right inset showing the same for vertically aligned twin Si-NWs after full conversion. Fin aspect ratios of about two and more result in twin wires. Fig. 2(c) shows a 1-D array of NWs. The large-area ordered mesh of NWs shown in Fig. 2(d) is an indication of the robustness of the process.

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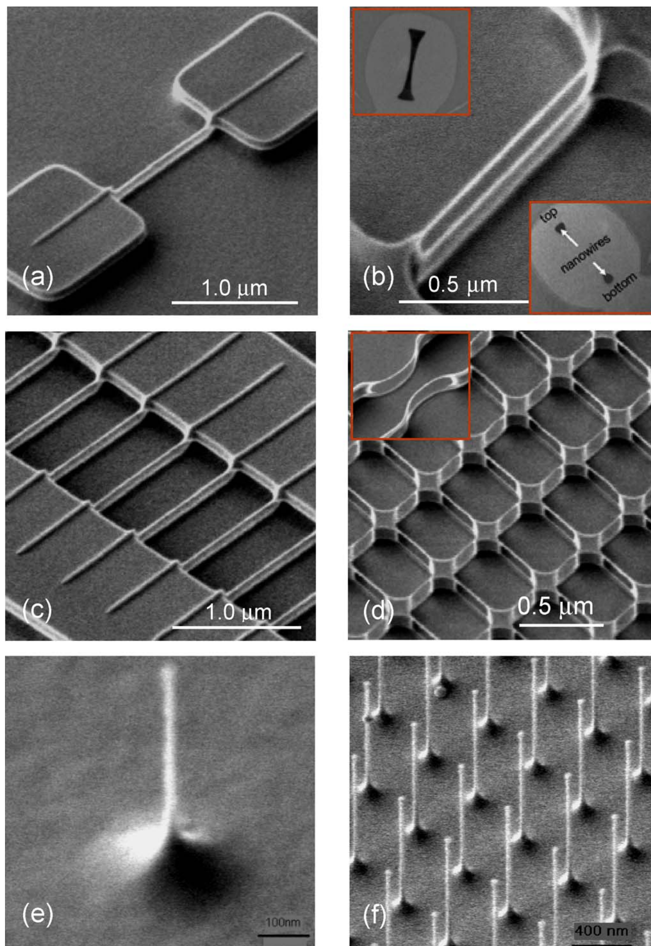

Fig. 2. (a) Single Si-NW. (b) Vertically stacked twin Si-NWs. The top inset shows the TEM cross section of a partially oxidized silicon fin indicating the mechanism; the center region is oxidizing faster and has become much thinner than the top and the bottom. The lower inset shows the TEM cross section of the twin NW embedded in oxide. (c) Array of Si-NWs. (d) Large-area regular mesh of NWs. The inset shows the curved NWs by the curved pattern defined using lithography. (e) and (f) 1.0-μm tall isolated and dense arrays of vertical Si-NWs of ~20-nm diameter, respectively.

The inset on the top-left corner shows the curved NWs obtained upon oxidation of curved silicon fins defined by lithography on a bulk wafer. Fig. 2(e) and (f) shows the SEM micrograph of isolated and dense array of vertical NWs fabricated using the same process sequence as lateral NWs.

By utilizing such NWs as channel body, we have fabricated GAA NW-FETs [28], NW-Schottky barrier FETs [30], SONOS-type NVM cells [31], and NW logic circuits. In our approach, the device and circuit fabrication is straightforward—very similar to the process steps used in standard CMOS flow. The gate oxide is grown or deposited on the NWs, followed by gate electrode deposition and definition. S/D implantation, metallization, followed by alloying complete the fabrication process similar to the planar FETs. The NW channel remains undoped, i.e., no intentional doping to adjust V_{TH} or to control short-channel effects is introduced. After NW formation, the key process is gate definition in which the dry etching process requires a high selectivity to gate dielectric.

Shown in Fig. 3(a) is the tilted view of the SEM image after gate definition. The TEM cross section across the NW channel is shown in Fig. 3(b), where ~3-nm-thick Si-NW and

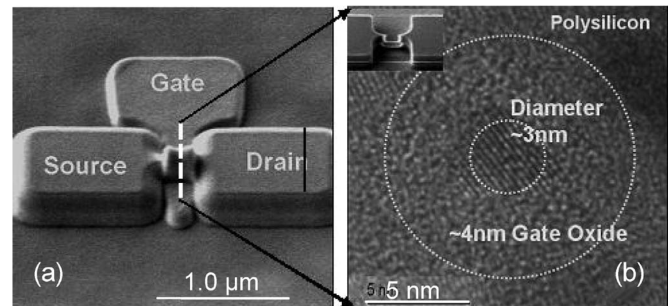

Fig. 3. (a) GAA NW transistor with gate length of 350 nm after gate patterning and (b) its TEM cross section in which ~3-nm-thick Si-NW surrounded by 4-nm SiO_2 followed by poly-silicon is clearly seen. The inset shows the NW channel before poly-gate deposition. Reprinted with permission from [29].

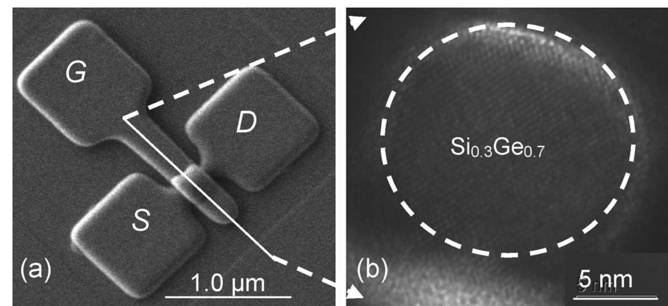

Fig. 4. (a) NW device after gate definition. (b) TEM cross-sectional image of the NW channel across the length. The Ge% is conformed using EDX. Reprinted with permission from [32].

4-nm-thick oxide are clearly seen to be surrounded with the GAA polysilicon. The tilted view of the SEM image of the wire channel just after gate oxidation is shown as an inset in Fig. 3(b).

The top–down fabrication has been extended to SiGe NW channels targeting high-speed requirements. Pattern-dependent Ge condensation (1-D condensation in wider S/D contact pads and 2-D condensation in the narrow fins) is observed during the oxidation process. This leads to heterojunction NW structures (S/D with 30% Ge and NW channel with ~70% Ge), which were integrated into a PFET, with HfO_2 as the high-k gate dielectric, along with TaN as the metal gate. Fig. 4(a) shows the tilted view of the SEM micrograph of the device after gate definition, along with the TEM cross-sectional image in Fig. 4(b) of ~13-nm-thick NW channel after complete fabrication. These Ge-rich NW PFETs in nearly GAA architecture show significant drive current enhancement vis-à-vis planar devices [32].

One of the issues with the NW-based devices is the low-drive-current capability per NW channel due to ultranarrow channel body which limits the total number of charge carriers. Increasing the number of NWs laterally helps increase the drive current but at the cost of increased consumption of silicon estate and increase in parasitic. Our group devised a novel approach by vertically stacking the NWs using SiGe as the sacrificial layer. The differential in oxidation rate between Si and SiGe leads to faster oxidation of SiGe as well as condensation of Ge onto the Si surface in the stack [33], [34]. Vertical stacking of NWs yields much higher drive current without any increase in the consumption of silicon estate. Fig. 5 shows the SEM images

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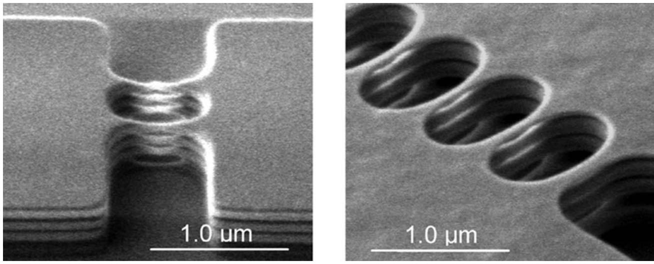

Fig. 5. Tilted view of the SEM images after release of the stacked NW. (Left) Two stacks of three-stacked NWs. (Right) Five stacks of four-stacked NWs. Reprinted with permission from [34].

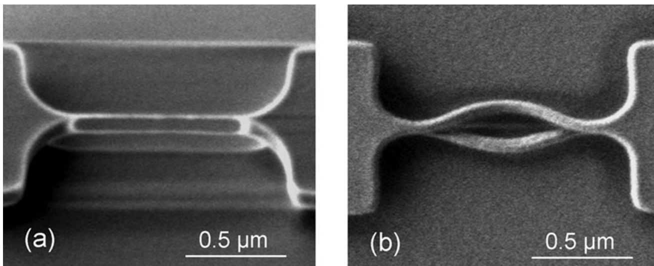

Fig. 6. Tilted view of the SEM images of the released Si-NWs of length 0.85 μm anchored on both sides (left) before and (right) after high-k and metal depositions. The wires are severely twisted in the opposite direction after metal deposition. Reprinted with permission from [35].

of the fabricated 2 × 3 (left) and 5 × 4 (right) stacked arrays of NW channels. Similar stacking using dry etching of sacrificial SiGe layer, followed by H_2, annealing has been reported by Ernst *et al.* [26].

We obtained interesting results related to the impact of stress on the physical structure of NWs when we fabricated high-k/metal gate GAA devices. Severe twisting of anchored Si-NW beams was observed once the tantalum nitride (TaN) metal was sputter deposited on the HfO_2-coated NWs [35]. The NWs maintained electrical continuity under estimated stress level of the order of ∼4 GPa, which originated from the stress in the deposited metal film. Fig. 6 shows the tilted view SEM images of the wires before and after metal deposition; severe twisting is clearly visible.

III. Electrical Characterization of NW MOSFETs

A. I–V Characteristics

Most of the reported data on the I–V characteristics of GAA NW FETs show excellent gate control, near-ideal subthreshold behavior, high I_{ON}/I_{OFF} ratio, and high drive current [21], [27]–[29]. For instance, we obtained I_{ON} values of 2.4 and 1.3 mA/μm, DIBL values of 8 and 13 mV/V, and SS of 60 and 65 mV/dec for NMOS and PMOS, respectively [29]. The I–V characteristics of these GAA Si-NW devices with 3-nm diameter are shown in Fig. 7, where the current is normalized to diameter. Although it is a matter of debate, it is worth mentioning here that the typical trend in the contemporary NW literature is the normalization to diameter, which may be appropriate only with fully volume-inverted channels existing in the case of ultranarrow undoped wire channels. With thicker wire where conduction remains at surface, it should be more appropriate to use perimeter for normalization. We have used normalization to diameter for wire diameters up to 10 nm. Above 10 nm, normalization to perimeter is performed.

The drive performance has been recently improved very significantly [36] by appropriate salicidation of S/D extensions and reduction of gate length to 8 nm; the NMOS drive current of 3.67 mA/μm is achieved with excellent gate control with 10-nm-thick wire channels.

Table I gives the comparative list of device electrical and structural parameters reported in the literature, along with the best reported FinFET performance.

The terminal characteristics of heterostructure PFETs (Fig. 6) are shown in Fig. 8. The heterojunction NW FET with NW of ∼13-nm diameter exhibits ∼4.5× transconductance and drive current improvements compared to the corresponding planar device. The enhanced hole injection velocity on account of heterojunction between the source and the channel, compressive strain, and high Ge contents (70%) in the channel are speculated as possible contributors to the improvement. Possible causes of low values of absolute current in the case of both the NW and the planar device could be not-so-good quality of interface between HfO_2 and SiGe channel body as well as on account of increased scattering due to alloyed Ge [32].

In Fig. 9, the transfer characteristics of the GAA NW FETs fabricated on vertically stacked NWs (Fig. 5) are presented. The device electrostatic behavior is as good as reported on single Si-NW channels in Fig. 7. Thus, our vertical stacking strategy leads to enhanced drive capability per silicon estate without compromising on the other performance parameters. The absence of g_m degradation in NMOS relative to that in PMOS points to confinement of electrons to the core of the wires and holes to the surface due to bandgap offsets between Si and SiGe sketched in the inset of Fig. 9 [34]. The SiGe surface is a result of Ge condensation into silicon during the oxidation process.

B. Carrier Transport in NW Channels

Characterization and modeling of carrier transport in the NW channels are paramount for applications of these devices in circuits as well as for physical understanding. The NW devices are usually undoped, and the short-channel effects are controlled using device architecture. The carrier transport in the undoped GAA NW channel is expected to be superior to that of the planar bulk FET due to reduced Coulomb scattering—fewer ionized dopants in the intentionally undoped NW channel. Due to the cylindrical symmetry, the surface electric field is higher in GAA FET, and that is expected to reduce the carrier mobility, specifically due to relatively rough surface made up of multiple orientations of the exposed crystal planes. In the case of ultrathin NW channels, however, most of the carriers remain in the core of the wire on account of quantum–mechanical effects and thus enjoy low vertical field and weak scattering. In view of the aforementioned factors, 1-D transport may have larger mean free paths of the carriers and, hence, higher mobility/ballisticity [40]. It will be therefore interesting to investigate the carrier mobility in NW FETs. However, the measurement of the ultralow capacitance of the NW channels is challenging, and not much data are reported using the measured C–V characteristics.

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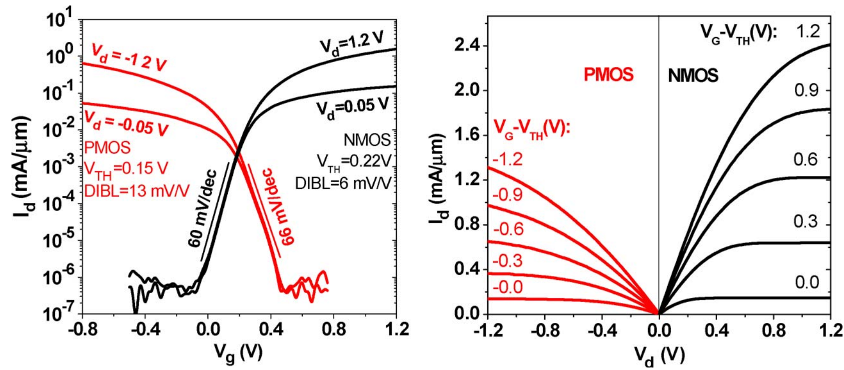

Fig. 7. (a) Transfer characteristics of GAA n- and p-FETs (Fig. 3: $L_G = 350$ nm and $T_{OX} = 4$ nm) showing near-ideal subthreshold swing indicating the excellent electrostatic control. (b) Drain current characteristics showing that high drive currents are possible in GAA FETs. Reprinted with permission from [29].

TABLE I
NW AND FinFET TRANSISTOR PERFORMANCE DATA

Device Type	Grown Nanowire		Top-Down Nanowire		Fin-FETs	
	N* [37]	P [38]	N [36]	P [27]	N [39]	P [39]
NW dia./Fin Width	20	15	10	8	25	25
Channel length (nm)	2000	40	8	15	40	40
Normalization method	diameter	diameter	diameter	diameter	W_{FIN}+2*H_{FIN}	W_{FIN}+2*H_{FIN}
I_{ON} (uA/um)	80	2100	3670	1940	1395	1140
I_{ON}/I_{OFF}	~10^4	~10^3	>10^6	>10^5	>10^4	>10^4
DIBL(mV/V)	-	-	28	43	89	101
SS(mV/dec)	300	140	73	71	76	82
V_{DD} (V)	5	-0.5	1	-1	1.1	-1.1

*I_{ON} data [37] is at V_{GS}=5V and V_{DS}=1V. W_{FIN} and H_{FIN} are is fin width and height respectively.

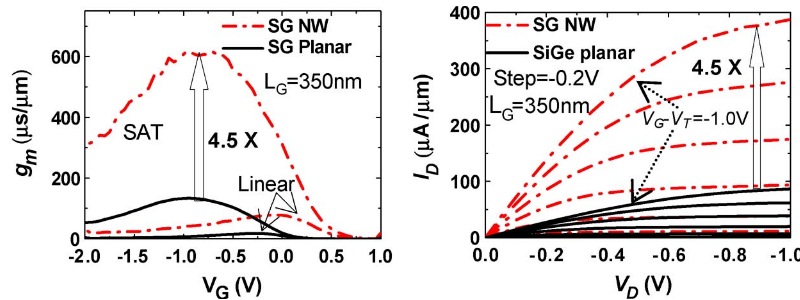

Fig. 8. (Left) Transconductance g_m and (right) output characteristics comparing the SiGe hetero-NW device (Fig. 4: $L_G = 350$ nm, NW diameter of $\sim$13 nm, and $T_{HfO_2} = 8$ nm) performance with that of the planar reference device. The current values are normalized to the perimeter of the wire. Reprinted with permission from [32].

Cui *et al.* [41] used the numerically simulated capacitance values, in conjunction with the measured I–V characteristics, to estimate the mobility in grown PMOS NW transistors, and estimated the peak hole mobility to be $\sim$1350 $cm^2/V \cdot s$ in 10–20-nm-thick Si-NW channels. Tu *et al.* [42] measured the C–V characteristics for grown Ge NWs with Schottky barrier S/D using special shielding arrangements on the probe station at low temperatures. The hole mobility value obtained was reported to be $\sim$400 $cm^2/V \cdot s$. Recently, Tezuka *et al.* [22] reported split C–V measurement on top–down omega-gated strained and unstrained Si and Ge NW devices by connecting about 500 device channels in parallel. Mobility enhancement by a factor of 1.6 for holes and 1.9 for electrons is observed due to the introduced strain. Suk *et al.* [43] reported a peak mobility value of 300 $cm^2/V \cdot s$ for holes and $\sim$200 $cm^2/V \cdot s$ for electrons from the C–V measurements of $\sim$10 000 GAA NW device channels in parallel. They reported an enhancement in mobility with reduction in NW diameter until 4 nm and a reduction in mobility below 4-nm NW diameter. The higher values of hole mobility compared to electron mobility were attributed to the presence of compressive stress in the channel due to Ge in S/D extension pads. Fig. 10(a) and (b) shows the mobility data from Tezuka *et al.* [22] and Suk *et al.* [43], respectively, plotted against NW diameter/thickness indicating a large scatter in mobility values and behavior.

The S/D access resistance is another critical parameter which needs to be extracted from actual devices and has been an issue in grown NWs due to the small volume of silicon in the contact

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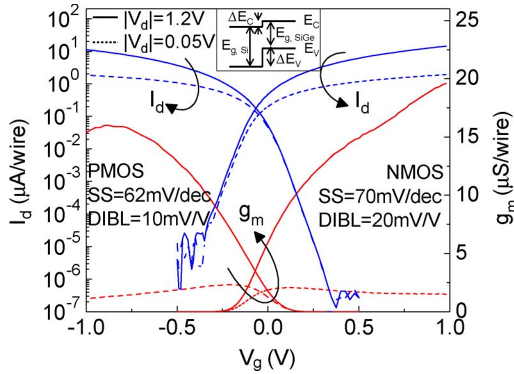

Fig. 9. Per-NW I_d-V_g and g_m-V_g plots for stacked NW n-FETs and p-FETs with $L_G = 500$ nm and NW diameter of ∼30 nm. Reproduced here with permission from [34].

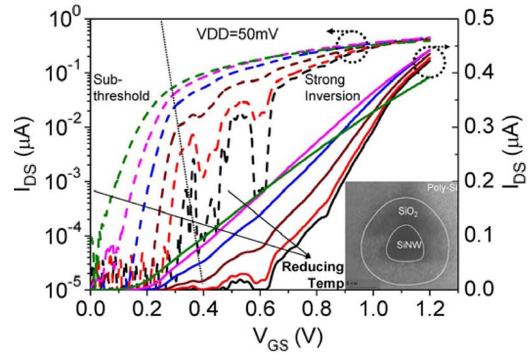

Fig. 11. Measured $I_{\rm DS}-V_{\rm GS}$ (at $V_{\rm DS} = 50$ mV) characteristics of ∼7-nm triangular Si-NW n-FET with effective gate length of ∼300 nm at different temperatures: 5 K, 37 K, 77 K, 137 K, 200 K, and 295 K. Reprinted with permission from [48].

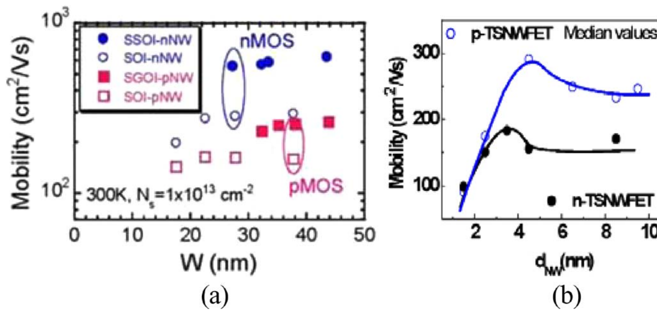

Fig. 10. Experimentally extracted electron and hole mobility values in NW FETs plotted against the NW diameter/thickness. (a) Is from [22] for the case of omega-gated NW FET, and (b) is from [43] for the case of GAA NW FET (reprinted with permission).

area. Recently, Suk *et al.* [22] reported the extension resistance in the range of 1.5–2 kΩ, which is at par with the planar bulk FETs [44].

C. Quantum–Mechanical Effects on Transport at Low Temperature

Electrical characterization of NW devices at cryogenic temperatures shows the evidence of discrete energy bands as a result of quantum confinement [45]–[48]. Discrete energy bands in conduction (valence) band have direct impact on the transport as well as the threshold voltage. Colinge *et al.* [45], [46] showed oscillatory g_m–V_G behavior in ultranarrow fin channels. We have observed oscillation in I_D–V_G characteristics and a reduction in drive current at low temperature, possibly on account of intersubband scattering of the carriers due to large energy separation in the subbands for NW channels with reduced diameters (7 nm), as shown in Fig. 11 [48].

IV. NW CMOS Circuits

The NW transistors are being projected for terahertz switching applications due to their good dc performance and extremely small gate-to-channel capacitance resulting in ultrasmall intrinsic gate delay (CV/I). However, the projected delays based on the dc characteristics of individual transistors and the estimated capacitance using an ideal structure are not always good indicators of the device performance while used in circuits due to the presence of various parasitics. The importance of the parasitic associated with the device structure becomes clearly evident only when the devices are evaluated in a circuit. For instances, although carbon-nanotube (CNT) devices are projected to be extremely fast devices, the first ring oscillator (RO) reported [49] using CNTs is slow, showing a delay of 1.4 ns due to the parasitic in the fabricated structures. The RO on plastic/glass using grown NW channels from the Harvard group [50] shows a stage delay of ∼14 ns, which increases by almost a factor of three on silicon due to increased parasitic. These devices use larger gate lengths (2 μm). For evaluating the performance of NW devices in circuits, we have fabricated and characterized the GAA NW CMOS inverter logic gates and ROs.

A. GAA Si-NW CMOS Inverters

We have demonstrated CMOS inverters with NW GAA channels using the top–down approach [51]–[54]. The symmetry in pull-up/pull-down characteristics has been achieved in two different ways, namely, 1) by using a longer n-channel device compared with the p-channel device [51] and 2) by using a larger number of NWs in p-channel transistors [52]–[54]. In both ways, the inverters performed with excellent gains, noise margins, and extremely low (a few nanoamperes) short-circuit current. Fig. 12 shows the tilted view of the SEM image of NW NMOS and PMOS transistors of the inverter with different number of channels in each device for symmetry. The insets in the figure show the corresponding wire channels before gate stack deposition.

Shown in Fig. 13(a) are the inverter dc characteristics. The inverters function well down to 0.2 V of $V_{\rm DD}$, which is an extremely good result for low-voltage/low-power applications. Fig. 13(b) shows the phase inversion characteristics of GAA NW CMOS inverters at 1 MHz. The inverter used for dynamic performance characterization comprised 20 n-channel and 50 p-channel NW MOSFETs.

Wang *et al.* [17] also reported CMOS NW inverters fabricated using the SNAP process. The circuit functionality was demonstrated, but the gain was poor. The inverters with grown NWs as the channel bodies and integrated on the glass/plastic substrate with long channel [50] show relatively better characteristics using high $V_{\rm DD}$ values (∼43 V). This performance may

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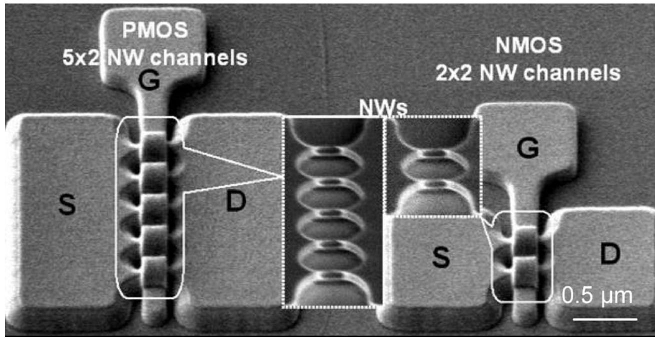

Fig. 12. Tilted view of the SEM image of NMOS and PMOS GAA NW transistors of the inverter logic after poly-gate definition. The channel length is 0.35 μm. The NW channels of ∼5–7-nm thickness are shown as insets.

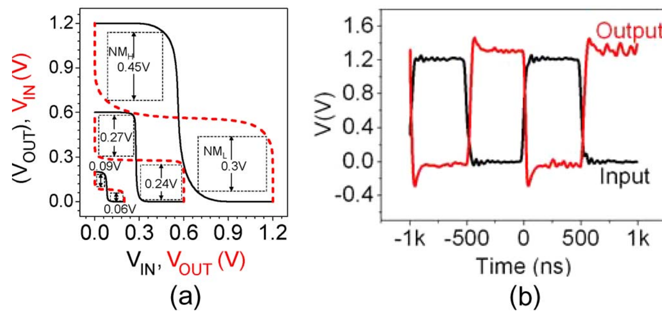

Fig. 13. (a) Transfer characteristics of inverter at different V_{DD}'s, with V_{IN} and V_{OUT} plotted interchangeably on the x- and y-axes (reprinted with permission). (b) Dynamic (pulse) response of an inverter with 50 pairs of PMOS channels and 20 pairs of NMOS channels at 1 MHz. The output levels clearly reach V_{DD}. $L_G = 0.35$ μm and $T_{\mathrm{OX}} = 5$ nm.

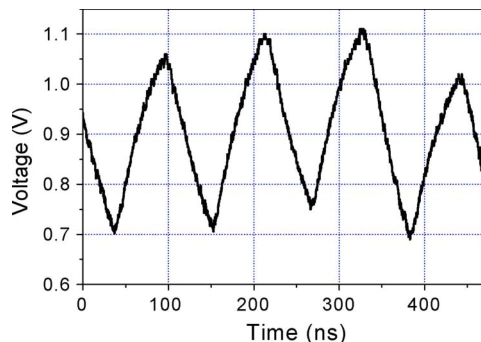

Fig. 14. 41-stage RO waveforms at $V_{\mathrm{DD}} = 1.2$ V. The frequency of oscillation is ∼8.8 MHz, $L_G = 0.25$ μm, and $T_{\mathrm{OX}} = 9$ nm.

have a possible application in stretchable/wearable electronics for grown NW device technology once the device structure is improved to bring down the required V_{DD} values.

B. GAA Si-NW CMOS ROs

ROs are the basic tools to characterize the digital performance of technology. We have fabricated and characterized 41-stage NW CMOS ROs using the top–down approach. The measured RO wave shapes are shown in Fig. 14. The wave shapes were picked up with the help of the active probe (Picoprobe model 35 with 50-fF input capacitance). The signal excursion does not traverse rail to rail due to the smaller size

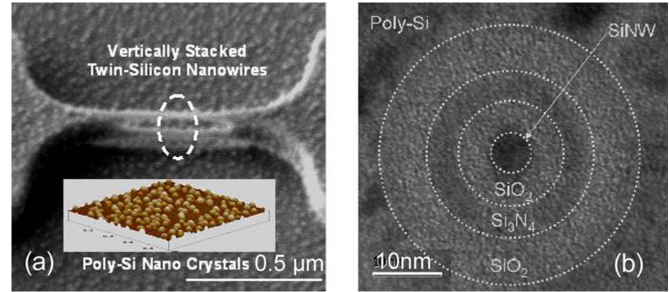

Fig. 15. (a) SEM image of twin-Si-NW channels after oxide, nitride, and poly-Si-NC depositions. The inset shows the AFM image of the nanocrystals. (b) TEM cross section of one of the NW channels across the wire length. Reprinted with permission from [61].

of the NW CMOS buffer at the output. The delay per stage is ∼1.4 ns, which is much higher than the best value reported (5.1 ps) using bulk planar FET [55] and 13.9 ps with FinFET [56] devices. Our delay is similar to those reported for CNT RO [49]. The typical delay for planar technology at 0.25-μm gate length, which is incidentally the gate length of the devices used in our ROs, is ∼40 ps [57]. The main cause of the larger delay in our case is the low drive current of the NW FETs due to very narrow channels (vis-à-vis 0.25-μm planar devices) and the parasitic capacitance due to the relatively long extension of gate polysilicon beyond the NW channel for gate contact. This extension region sits over a thin buried oxide (less than 0.15 μm in thickness) in our structures. We believe that increasing the buried oxide thickness and implementing the salicidation process [36] will significantly improve the RO performance.

V. NW NVMs

Floating-gate NVM has two major limitations that impact the integration density, namely, 1) neighboring cell interference and 2) short-channel effects. Multiple-gate devices in SONOS architecture [49] relax these limitations very significantly. The SONOS structure is inherently immune to neighboring cell interference [58], while the multiple-gate structures help overcome the short-channel effects. Thus, NWs in NVM are poised to increase the density of integration to ultimate scaling limit.

In addition, the radial field distribution in cylindrical GAA structures indicates high concentration of field at the silicon/tunneling oxide interface compared to that in the blocking oxide [31]. In the case of a 5-nm-diameter Si-NW channel, we find that the cylindrical geometry enhances the electric field at the Si–SiO_2 interface by approximately three times with respect to the planar structure with the same dielectric thickness (ONO: 4.5nm/4.5nm/9nm). Also, the GAA device leads to lower electric field in the blocking oxide, i.e., far away from the axis of the cylinder. This helps in using Fowler–Nordhiem (F/N) tunneling as the preferred mode of programming and erase.

We fabricated a SONOS-type NVM cell with and without trap layer engineering (TLE) using the top–down approach. Fig. 15(a) shows the SEM image of vertically aligned twin-Si-NW channels after tunnel oxide (4.5 nm), trap nitride (4.5 nm), silicon nanocrystals (Si-NCs), and blocking oxide (8 nm)

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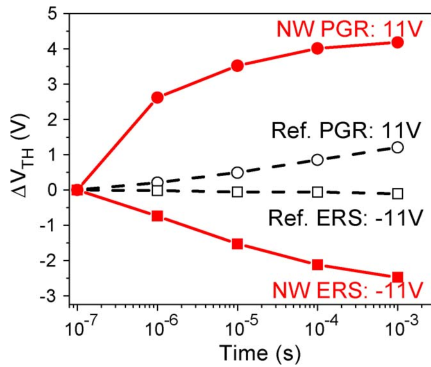

Fig. 16. Comparison of P/E characteristics of the vertically stacked twin-Si-NW SONOS memory cell (gate length of 850 nm; NW diameter of ∼5 nm; ONO: 4.5 nm/4.5 nm/8 nm) with that of the reference planar device ($W = 5\ \mu$m). In all cases, the pulse is applied at the gate while keeping the S/D at ground potential for F/N tunneling. Reprinted with permission from [31].

depositions using LPCVD processes. The inset shows the AFM image of the Si-NCs which were deposited over the nitride layer for trap engineering used to enhance the program and erase (P/E) efficiency, as discussed in the following paragraph. The TEM image of the cross section of one of the NW channels is shown in Fig. 15(b). The NW and all the surrounding layers (O–N–O–poly-Si gate) are clearly seen.

Fig. 16 shows the typical P/E characteristics of the vertically stacked twin-Si-NW SONOS memory cell, along with those of a cofabricated planar device [31]. Based on the programming characteristics, the NW-NVM cells exhibit a large V_{TH} shift of 2.6 V for a 1-μs programming pulse of +11-V amplitude compared to insignificant V_{TH} change in the case of the planar device for the same programming conditions. The erase characteristics also show that the NW-NVM devices are much faster than their planar counterparts. The NW-NVM cell requires 1-ms time to erase the charge written in 1 μs. The slow speed of the erase process is known to be due to the lower tunneling probability of holes used in the erase process compared with that of electrons involved in programming.

The P/E speed of the NW-NVM cells presented here is faster than the omega-gated rectangular-shaped NW SONOS [59] and complements the work by Suk *et al.* [60] on twin-Si-NW GAA SONOS memory cells.

Furthermore, as mentioned previously, we obtained significant improvement in P/E speed and memory window by depositing Si-NCs on the trap layer. The nanocrystals provide additional accessible sites with an effective deeper trap energy level, which trap and detrap more carriers with higher efficiency. Utilizing this engineered trap layer, for the same P/E conditions, the threshold voltage shift improved to 3.2 V with a total P/E window of 6.25 V [61]. Thus, the NW-based SONOS cell appears to be a potential candidate for future high-speed, low-voltage, and high-density NAND-type nonvolatile flash memory applications.

VI. More-Than-Moore Regime

In this section, we discuss the use of Si-NWs as chemical/biochemical sensors. Biosensing by Si-NW is based on depletion or accumulation of charge carriers in its "bulk" when charged biomolecules are bound to its surface. When the depletion or accumulation width in the NW is comparable to its cross-sectional dimension (at higher surface-to-volume ratio), pronounced conductance changes are observed, leading to high sensitivity for chemical/biochemical sensing. Electrical sensing through change in conductance (or resistance) of Si-NW has been demonstrated successfully for metal ions [9], [10], [62], DNA [63]–[68], proteins [69]–[71], virus [72], and cells [73]. Such electrical sensing allows easier miniaturization of biodetection platforms with electronic readout (replacing more bulky optical scanners as used in conventional fluorescence-based detection). This can lead to portable and handheld medical diagnostic devices in the future. As Si-NWs can be fabricated in large array formats, there exists a huge potential for simultaneous analysis of multiple species on a sensor chip backed by electronic readout and data acquisition systems which would facilitate complex disease diagnosis.

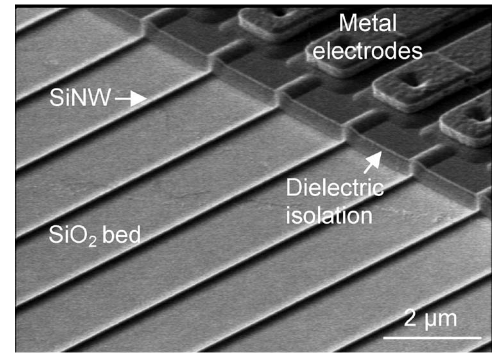

Fig. 17. Si-NW array fabricated by the top–down fabrication technology for biosensing applications. Reprinted with permission from [66].

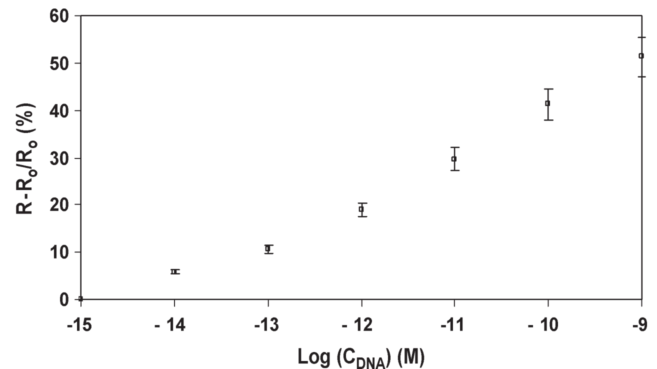

Fig. 18. Response of the PNA-functionalized Si-NWs to target the DNA of different concentrations. Reprinted with permission from [66].

Fig. 17 shows the SEM photograph of a Si-NW array fabricated with the top–down approach with the capability of electrically measuring each wire individually. In our sensing studies, the typical width of Si-NW is 30–60 nm with 100-μm length. The NWs are supported mechanically at the bottom by the SiO_2 BOX layer (called as bed) of an SOI wafer.

Fig. 18 shows the fractional change in the conductivity for DNA sensing as a function of its molar concentration after surface functionalization and subsequent binding of the target molecules. Detection of a few tens of femtomolar concentration

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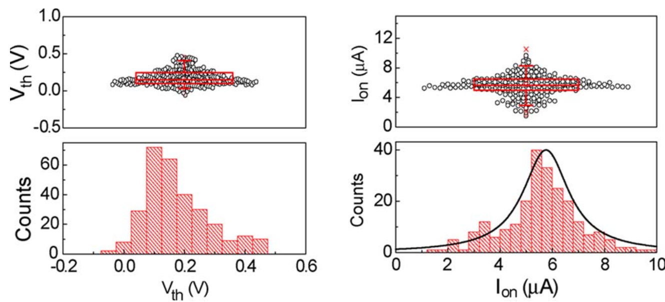

Fig. 19. (Left) NMOS $V_{\rm TH}$ box plot and histogram. The $V_{\rm TH}$ for the majority of devices lies between 0.12 ± 0.05 V. (Right) NMOS $I_{\rm ON}$ box plot and histogram. The $I_{\rm ON}$ for the majority of the devices lies between 5.5 ± 0.5 μA. The NW thickness is from 3 to 6 nm. Reprinted with permission from [29].

demonstrates very high sensitivity of these devices [66]. Sensitivity can be enhanced further with reduced SiO_2 thickness on top of wires, similar to the case of a classical FET, as the charges from the attached biomolecules (gate charges) are closer to the Si-NW surface for better sensing [67].

VII. Challenges and Opportunities

There has been significant progress in fabrication technology, and in understanding of the electrostatics and transport in the GAA NW devices, huge challenges remain to be met before this new device architecture reaches the level of manufacturing. The first challenge is large device parameter variability in the threshold voltage and $I_{\rm ON}$, as shown in Fig. 19. This variability is mainly attributed to possible variation of NW shape and size/diameter and variation in interface quality. Tight control of the starting fin dimensions with advanced lithography and shape control using H_2 annealing may help in reducing this variation. The high sensitivity of device parameters, particularly the $V_{\rm TH}$ to NW size, could possibly be attributed to the variation in silicon-channel-to-oxide-interface quality and change in bandgap as a result of quantum confinement effects [74]. Variation in surface roughness could be the possible reason for $V_{\rm TH}$ fluctuations, as an increase in $V_{\rm TH}$ with surface roughness is speculated [75]. Probabilistic circuit design techniques could form part of the solution for the successful implementation of GAA NW devices into manufacturable circuits.

The second challenge pertains to the tuning of the threshold voltage. Due to the very limited volume of channel body, the doping of the channel for $V_{\rm TH}$ adjustment is not feasible. Due to the cylindrical architecture, the impact of gate oxide thickness on $V_{\rm TH}$ is also expected to be significantly diminished. The feasible solutions lie with the tuning of the gate electrode work function and the wire diameters.

The third challenge is in terms of integration density which is limited by lithographic resolution in the case of top–down CMOS-compatible NWs. However, we believe that with advances in lithography, the integration density of top–down NWs will keep on increasing and may match the extremely high density projections using the bottom–up approach. For high drive currents, as needed, for example, in pad drivers, vertical stacking of NWs could be a solution as that would reduce demand on silicon estate. Another possible option could be the use of grown NWs for increasing the drive current/device density once the daunting challenges of their manufacturable assembly in circuit functionality are met successfully.

VIII. Conclusion

The status of GAA NW CMOS technology using the top–down approach has been reviewed. The top–down approach is highly integrable in circuit functionality and is compatible with the existing CMOS technology. NWs and nanostructures seem to have possible novel solutions in the "more-than-Moore" regime of applications such as in the area of fabrication of chemical/biochemical sensors. The presented top–down techniques can potentially address the needs of the "end-of-the-technology roadmap" and beyond CMOS era, possibly with the help of a hybrid approach. Thus, the NW technology indicates feasibility of opening up newer application opportunities for Si technology.

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