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Integration of High Aspect Ratio Tapered Silicon Via for Through-Silicon Interconnection

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Abstract

This paper provides a detailed overview of silicon carrier based packaging for 3D system in packaging application. In this work the various critical process modules that play a vital role in the integration and fabrication of silicon carrier with high aspect ratio tapered through-silicon interconnections have been explained and discussed with experimental data.

A method of fabricating tapered deep silicon via in a 3-step approach has been developed and characterized which controls via depth, sidewall profile and surface roughness effectively. A low-temperature dielectric deposition process is also developed that has minimum residual stress and good dielectric coverage on the via sidewall. The above processes were then integrated with back-end processes like seed metallization, copper electroplating, chemical mechanical polishing and wafer thinning to realize a fully integrated silicon carrier fabrication technology. The silicon carriers were finally assembled and tested for through silicon interconnection.

Introduction

Through-silicon interconnection technology is an enabling technology for three dimensional chip integration and system in packaging (SIP) application. It provides vital solution to the performance bottleneck associated with traditional and inherently long two dimensional chip-to-chip interconnections thus leading to obvious space saving and reduction in power dissipation and power consumption [1].

A preferred approach for vertical integration of known good electronic and MEMS devices is by using a silicon interposer or silicon carrier with through silicon interconnections. It also enables vertically integration of dissimilar or heterogeneous chips of different technologies. The heterogeneous devices are first integrated on the silicon carrier in 2D fashion. The silicon carriers are then vertically integrated by means of the through silicon interconnections as illustrated in figure 1. Such an integrated module is also known as silicon carrier-based package [2]. Silicon carrier based 3-D packaging is an extension of traditional 2-D chip integration as in multi-chip modules (MCM) [3]. The main merit of this type of packaging is that it allows known good dies to be assembled in each carrier. The individual carriers are further tested before stacking them vertically. Thus, this 3D architecture is not only cost-effective but also highly testable at each stage.

Another Market segment which requires vertical device integration is the micro electro-mechanical systems (MEMS) market which requires sensing functions to be integrated with semiconductor chips which is also known as application specific integrated circuits (ASICs). The MEMS devices

further requires encapsulation which can now be accomplished by using an active silicon chip as an encapsulating cap. Integration of MEMS with ASICs can now be achieved by vertical stacking of MEMS over the ASICs or vice versa [4].

Figure 1 below shows a generic 3D system in package (SIP) platform in which dissimilar chips and device are assembled in each silicon carrier and then stacked vertically. The silicon carrier is first fabricated at wafer level with through-wafer copper interconnections with suitable electrical isolations and copper diffusion barrier structures. The choice of the substrate and its specification such as resistivity is decided based on its application.

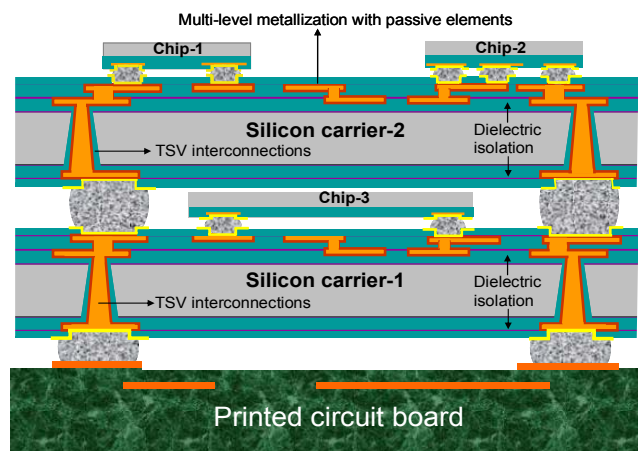


Figure-1: Illustration of 3-D SIP platform formed by stacking silicon carriers with through-silicon copper interconnections. Carrier thickness can typically be in the range of 200-300 μ m.

The main objective of this work is to address various critical technology challenges associated with integration of high-aspect ratio through silicon via (TSV) to form a reliable through-silicon interconnect structure by deep damascene copper via filling, CMP and finally by wafer thinning process. It is also the objective of this work to integrate the TSV structure for silicon carrier fabrication. Though there are a wide range of techniques for forming high aspect ratio deep silicon via structures like Bosch etch process [5], cryogenic etch process [6], laser drilling [7] and powder blast micromachining [8], these methods in its original form yield extremely vertical profiles which makes them less suitable for realizing a reliable void-free through silicon interconnection. The main challenges that needs to be addressed are to achieve (a) smooth via sidewalls, (b) uniform deposition of dielectric isolation layer over the via sidewall, (c) continuity of copper

diffusion barrier and copper seed metallization and (d) void-free copper electroplating. As the aspect ratios of deep silicon vias continues to increase it becomes more challenging to accomplish any of these requirements without making modifications to via profile. The approach adopted in this work is to gradually taper the via profile to mitigate the problems associated with plasma enhanced chemical vapor deposition (PECVD) and physical vapor deposition (PVD) processes which are ion-assisted processes and hence tend to yield non-conformal film deposition. Via profile tapering furthers helps in accomplishing a void-free copper electroplating process [9].

Experimental plan

Silicon carrier with normal resistivity $<100 \Omega\text{-cm}$ is suitable for application below 5GHz [10]. However, for higher frequency application, we may need a higher resistivity substrate. In the present work, a substrate resistivity of $< 100 \Omega\text{-cm}$ has been chosen. Following are the key process modules that need to be integrated to fabricate a silicon carrier with through silicon via (TSV) interconnections:

- Deep-silicon tapered via etch process: The tapered via is evolved in three stages. Each stage has to be independently optimized and characterized to achieve the final via process.
- Via sidewall dielectric isolation process: A low-temperature (250°C) plasma enhanced chemical vapor deposition (PECVD) process is developed and characterized for providing low-stress dielectric isolation structure for the through silicon via (TSV).
- Uniform deposition of copper diffusion barrier and copper seed metallization and final via-fill by copper electroplating process
- Chemical mechanical polishing (CMP) of overplated copper to form a damascene copper via.
- wafer back grind and polishing to form through silicon copper interconnection.

As a detailed study from (a) to (e) is beyond the scope of this work, the present study focuses on (a) and (b) only and the various process integration challenges are addressed.

Silicon carrier design

As explained earlier, the present work focuses on silicon carrier fabrication by via-first approach. Design of test dies and silicon carriers chips is shown below in figure 2 for electrical and reliability testing of vertically assembled samples. A $200\mu\text{m}$ thick silicon carrier with electrical continuity test structures with $50\mu\text{m}$ diameter via has been targeted by via-first approach. The aspect ratio for tapered silicon via targeted in this study is ≥ 3 . The through silicon vias are designed as peripheral vias with redistribution metal traces to interconnect the daisy chained test chips as shown below in figure 2. The continuity of the through silicon vias are tested by electrically probe-testing the organic substrate on which the silicon carriers are assembled as shown in figure 1.

Silicon carrier fabrication technology

The silicon carrier fabrication technology is described in some detail in this section as it is the focus of this work.

Figure 3 shows greater details of the silicon carrier wafer with through silicon interconnections shown in figure 1.

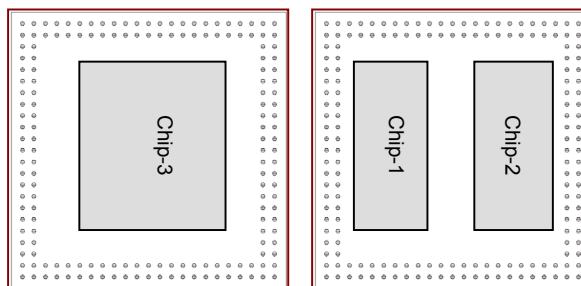


Figure-2: Layout of through silicon vias on silicon carriers for evaluating the TSV

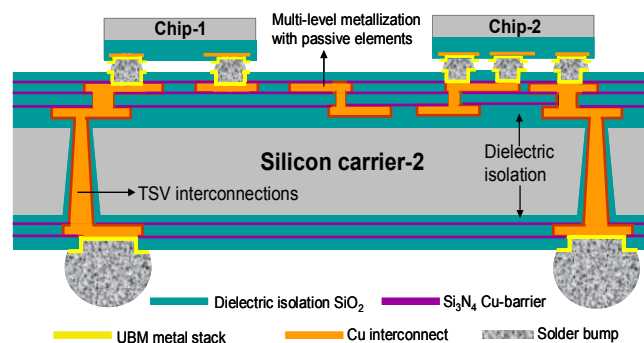


Figure-3: Detailed illustration of the silicon carrier with TSV used in the 3-D SIP platform.

The silicon carrier fabrication technologies can be broadly classified into two approaches namely (i) the via-first and (ii) the via-last approach. In the via-first approach, the required numbers of TSVs are fabricated as blind vias with the dielectric isolation and barrier/seed metallization before performing copper electroplating and chemical mechanical polishing (CMP) process. After performing the copper CMP process the multi-level metallization and RF passive elements are fabricated till the final passivation and UBM metallization. The carrier wafer is then attached to a handler wafer and back grinded and polished till the TSV structures are exposed from backside. Again multi-level metallization traces are formed similar to front-side of the carrier wafer till UBM metallization. The handler wafer is now released and separated from the front-side.

In case of via-last approach, the multi-level metallization and RF passive structures are first formed and then the front-side of the wafer is attached to a handler wafer and back grinded to $200\mu\text{m}$ thickness. Through silicon via structures are then formed to stop on front-side metal pads. The sidewalls of the through silicon vias are then deposited with dielectric isolation, barrier and copper seed metal layer. The vias are then filled by electroplated copper. The over-plated copper is removed by CMP process. The exposed TSVs are further redistributed by multi-level metallization. Finally, the backside metal pads are passivated and then patterned to form UBM metallization. The handler wafer is then separated. The process details are summarized below in table 1.

Table-1: Process flow summary for evaluation of silicon carrier fabrication technologies

Via-first		Via-last	
1	Blind via formation by DRIE	1	Front side multi-level metallization till Final passivation and UBM metallization
2	1 μ m PECVD SiO ₂ deposition	2	Handler wafer attachment on front-side
3	1KA Ti+1 μ m Cu seed metal deposition	3	Wafer thinning to 200 μ m
4	Cu-Electroplating & CMP process	4	Through silicon via formation by DRIE
5	Front side multi-level metallization till Final passivation and UBM metallization	5	2 μ m PECVD SiO ₂ deposition and etch back
6	Handler wafer attachment on front-side	6	1KA Ti+1 μ m Cu seed metal deposition
7	Wafer thinning to 200 μ m	7	Cu-Electroplating & CMP process
8	Backside multi-level metallization	8	Backside multi-level metallization
9	Passivation deposition, Pad open & UBM formation	9	Passivation deposition, Pad open & UBM formation
10	Handler wafer separation	10	Handler wafer separation

The fully fabricated silicon carriers are then used as a substrate for assembling known good dies and passive components as shown in figure 3. It may be noted that the handler wafer mentioned in both the approaches are attached by a temporary adhesive which is finally removed in the last step to detach the processed silicon carrier wafer [11]. A detailed study of thin wafer handling process is beyond the scope of the present work. The present work therefore focuses only on carrier fabrication by via-first approach.

Development of high aspect ratio tapered silicon via

The deep silicon via etch process development is done in inductive coupled plasma (ICP) based deep reactive ion etching system from Surface Technology System (STS). Although STS ICP system is mainly designed for performing deep reactive ion etch of silicon by a specially designed switched etch and passivation process, also known as BOSCH process, it can also be used in reactive ion etch mode, referred as non-BOSCH process in this paper. The system consists of ICP electronics, loadlock and carousel wafer loading unit and a process chamber. The plasma is generated by coil assembly which is inductively coupled at 13.56 MHz via the matching unit in a ceramic plasma chamber. This provides high density plasma capable of achieving high etch rates with little substrate damage. Independent biasing of platen is made available by a separate 13.56 MHz RF biasing circuit at the bottom electrode that comes with automatic power control and impedance matching. Process gas is introduced to the chamber through the upper electrode assembly. Wafers are clamped by electrostatic chuck (ESC) on the lower electrode which is powered at 13.56 MHz. The platen temperature is kept at 10°C by using re-circulating de-ionized water through a chiller system.

The via formation process is split into three independently controlled process steps, viz., (a) the straight via formation

step by BOSCH etch process, (b) via tapering process by a controlled isotropic etch process and (c) corner rounding etch process by a global isotropic etch process.

The straight via etch step is done to only 20-30% of the via depth. The first etch step defines the bottom region of the via structure. As the BOSCH etch process is based on cyclically switching between the SF₆ + O₂ based etch chemistry and C₄F₈ based deposition chemistry, it requires a good balance between the two to prevent accumulation of silicon grass due to the micro-masking effects of excessive fluorocarbon polymerization from C₄F₈. Typically, BOSCH process yields a very high anisotropy, and therefore one can expect deep vias with little tapering as shown in figure 4(a) for a 200 μ m deep via. A vertical profile however is highly undesirable for dielectric deposition, sidewall metallization by seed layer and via-filling by copper electroplating process.

In the second etch step, the remaining depth of the via is etched with a controlled isotropic etch process. The objective of this etch process is to slope or taper the sidewall of the deep silicon via to facilitate uniform deposition of dielectric, barrier and seed copper layer. It also helps in achieving a void-free copper via-filling by Cu-electroplating process. The via tapering is accomplished by introducing a controlled isotropic etch chemistry consisting of SF₆, Argon (Ar) and O₂ plasma immediately after the initial straight etch process. The second etch process being rich in F and SF_x-free radicals, needs sufficient oxygen to control excessive sidewall etch. Alternatively, C₄F₈ can be used to control excessive lateral etch [12]. The process pressure is maintained 30 millitorr to allow the reactants to create sufficient taper at the top while at the same time the bottom of the vias is not widened significantly. Figure 4(b) shows the cross section of the tapered via. It may be seen that due to the slight isotropic nature of the process, despite inhibition of the sidewall reaction, there is a slight curvature formation below the photo resist etch mask. The value of the curvature varies between 1-5 μ m depending on the diameter of the via and the slope of the photo resist mask (See figures 4(b) and 5(b)).

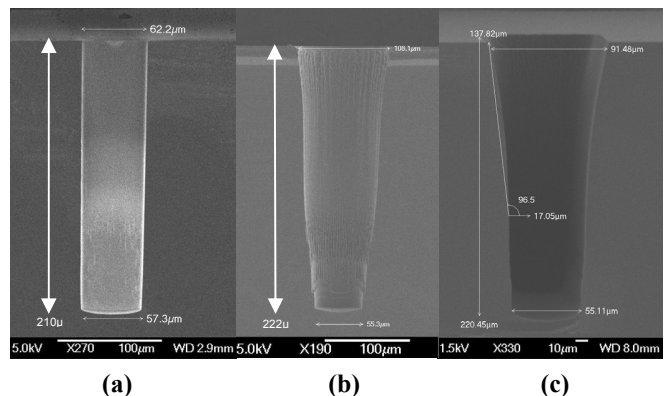


Figure-4: (a) Shows results achieved after 50 μ m diameter vias are etched to a depth in the range of 200-220 μ m. (b) Shows the evolution of a tapered profile after etch by a controlled isotropic etch process. (c) Shows the final tapered via profile after the top corner is rounder by a global isotropic etch process.

Table 2: Summary of the 3-step via tapering process.

Step-1- Straight etch process : BOSCH etch process	Etch cycle: APC: 77% (26mt); 130sccm SF ₆ ; 13 sccm O ₂ ; 600W Coil/ 20W Platen/ 6 sec.
	Passivation cycle: APC 77% (17mt); 85sccm C ₄ F ₈ ; 600W Coil; 5 sec.
	Platen Temperature: 10 °C Total process time: 30 minutes Etch rate: 3-3.5µm/min on 15-20% exposed area.
Step-2-Via tapering process: <i>Non-BOSCH or RIE process</i>	APC:78% (30mT); 84 sccm SF ₆ ; 67 sccm O ₂ ;59 sccm Ar ; 600W Coil power; 30W Platen power Platen Temperature: 10 °C Process time: 60min. Etch rate: 3.5-4.0µm/min on 15-20% exposed area.
Step-3-Via corner rounding process: <i>Global isotropic etch process</i>	APC: 65% (12-13mtorr); 180 sccm SF ₆ ; 18 sccm O ₂ ; 600W Coil power; 30W Platen power; Platen Temperature: 10 °C; Process time: 10 minutes. Etch rate: 1.5-2.0µm/min on blanket silicon wafer.

The photo resist mask is now stripped and the third etch step is performed to remove the defects created by the first and second etch processes. This is a global isotropic etch process consisting of largely directionless and neutral free radicals which causes the etch to be more at the top and gradually lesser at the bottom of the silicon via thus giving a tapered via profile. Having a low anisotropy is particularly important in this process as high lateral etch rate is required for removing the beaks or curvature formed due to the earlier two etch steps, and also to increase the amount of tapering at the top of vias. Figure 4(c) shows the final tapered via profile after the corner defect removal etch step. Table-2 below summarizes all the etch steps and corresponding gas chemistries used in the via fabrication process. Figure 5(a) shows the sidewall roughness immediately after the first etch step. Figure 5(b) shows the modified sidewall profile after performing the via tapering process. Figure 5(c) shows the final sidewall profile after the global isotropic etch process.

The global isotropic etch process was then further characterized to identify the critical process parameters that impacts the outcome of the tapering process viz, the taper angle and surface roughness due to global isotropic etch. Accordingly, the following critical parameters like etch gases, platen power and process pressure were varied and its tapering effect studied on via diameters from 10-100µm. The experimental matrix and its results are summarized in Table-3 and 4 below. Figure 6 is a plot showing the interaction between recipes#1 to 4 and the via tapering characteristics.

As the deep silicon via tapering is done globally on unprotected silicon surface, therefore it has the potential to increase the surface roughness of the silicon carrier if the process is not optimized. The via tapering and surface roughness study was done by keeping a fixed etch duration of 10 minutes and the surface roughness of silicon was measured

after each of the four etching condition. Each etched sample was scanned in Atomic Force Microscope and its average surface rough (Ra) was measured in nanometer (nm). Dimension 5000 scanning probe microscope system from Veeco Instruments was used to conduct the measurements. A 5nm by 5nm square area was scanned with a scan rate of 1.507 Hz outside the silicon via in the centre and edge of the wafer. The average value of the surface roughness has been tabulated in the last column of Table-3 for various isotropic etch process conditions. The trends from the table can be used for further optimization, if needed.

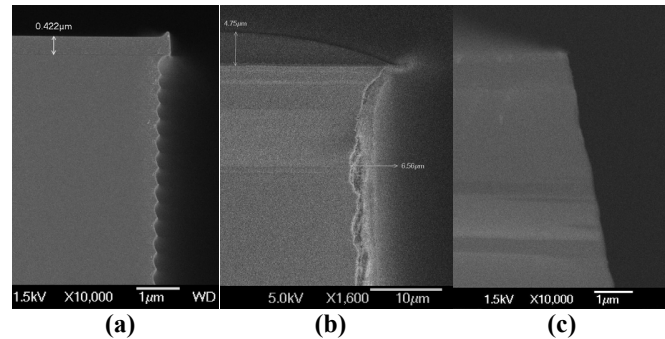


Figure-5: Optical micrographs showing via after performing the via tapering process on vias formed by (a) BOSCH and (b) non-BOSCH etch process.

Table-3: Taper etch process parameter matrix to study the impact on via slope and via diameter

Rcp #	SF ₆ (sccm)	O ₂ (sccm)	Ar (sccm)	Coil Power (W)	Platen Power (W)	Pressure (mtorr)	Surface Roughness (nm)
1	180	18	0	600	30	13	0.585
2	250	25	30	600	20	32	10.1
3	180	18	0	600	30	35	0.965
4	250	25	0	600	30	20	1.041

Table-4: Effect of global isotropic etch process parameters on via taper angle after etching for 30 minutes.

Via diameter (µm)	Via taper angle in degrees			
	Rcp#1	Rcp#2	Rcp#3	Rcp#4
10	99.5	103	100.3	101.9
20	99.6	99.6	98.3	99.1
30	98.1	98.7	97.1	99
40	97.9	97.9	98.4	97.8
50	97.4	96.9	95.7	97.2
60	97.3	95.8	94.3	96.4
70	95.7	95.6	93.3	95.7
80	95.5	94.8	93.2	96
90	94.7	94.1	92.8	94.4
100	95.1	94.3	92.5	94.2

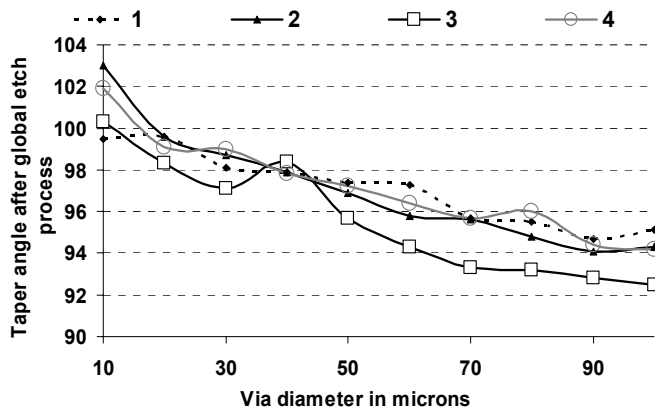


Figure-6: Graph showing the effect of various global isotropic etch process parameters on the taper angle.

Development of Low-temperature dielectric deposition

After the deep silicon vias have been formed, the vias are required to be electrically isolated by a uniform dielectric isolation layer. Normal process temperature for dielectric deposition by plasma enhanced chemical vapor deposition (PECVD) is 350-400°C. However, to prevent stress from accumulating in the silicon carrier wafer, a low-temperature plasma enhanced chemical vapor deposition (PECVD) process was developed. A low-temperature PECVD deposition process is needed not only for through silicon via isolation but also for dielectric isolation between redistribution layers on both sides of the carrier substrate. The temperature for the deposition process was chosen as 250°C as it is below the glass transition temperature of polymers glue use for thin wafer handling and also for the benzo-cyclo butane (BCB) polymer which is used as inter-metal dielectric in some process schemes.

Recipe Parameters	Parameter settings
Temperature	250 °C
Pressure	900 mTorr
Power	20 W
SiH ₄	6 sccm
N ₂ O	400 sccm
N ₂	150 sccm
Deposition rate	569Å/min
Uniformity	5.6 %

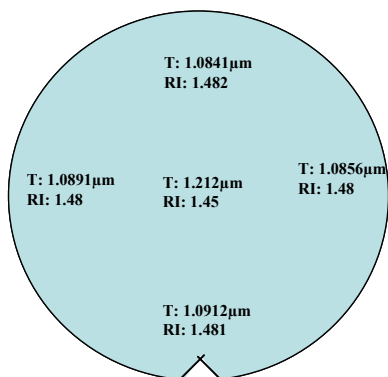


Figure-7: Low-temperature SiO₂ deposition process conditions in Plasmatherm-790 system and the wafer map showing the thickness and refractive index uniformity across the 8-inch wafer.

The proposed PECVD SiO₂ process was developed in Plasmatherm-790 dual chamber deposition/Etch system. The dielectric thickness used for the initial evaluation was 1.0μm. Actual thickness used for deposition and etch-back process is 2.0μm. The sidewall deposition uniformity was characterized in Jeol field emission SEM (JSM6700F) after completing the copper seed metallization and copper via filling by electroplating process. The sample wafer was cut through the

via structures and polished in lapping tool to get a smooth surface. The sample was further dipped in buffered oxide etchant (BOE) for 10 seconds to etch the sidewall oxide and decorate the various interfaces. Figure 8 below shows the cross section image of deep silicon via structure showing the sidewall oxide thickness achieved in the low-temperature deposition process which is adequate to achieve a very good dielectric isolation for electrical interconnections. Figure 8 shows the cross section SEM images of fully electroplating silicon via after low-temperature sidewall oxide deposition. It also shows the thickness achieved at top, middle and at the base of the via. The minimum thickness achieved is 0.35-0.45μm and maximum thickness achieved at the top sidewall is 0.7 to 0.8μm.

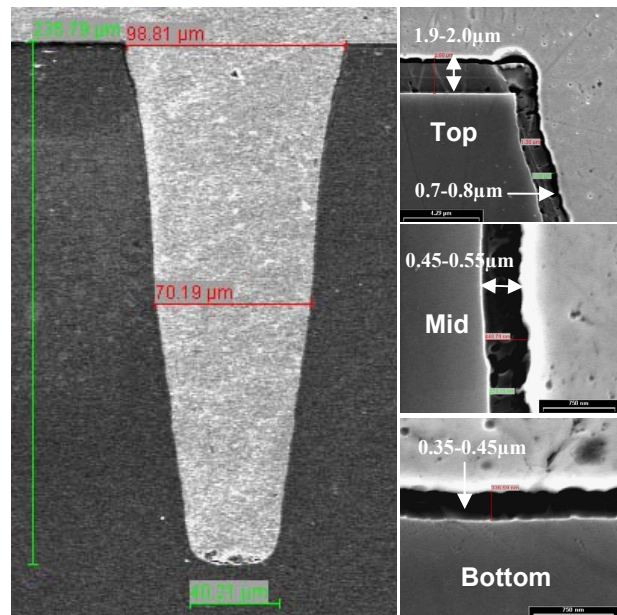


Figure-8: SEM image showing the void-free electroplated copper via structure and the thickness achieved for low-temperature PECVD oxide deposition process at top, middle and bottom of the vias.

Copper via-filling process

According to the curvature enhanced accelerator coverage (CEAC) mechanism proposed for copper damascene electroplating process [13, 14], the void-free filling of high aspect ratio vias occurs in following steps:

- Adsorption of additives & nucleation of electroplated copper on PVD films at a high over potential;
- Conformal growth of copper during initial deposition and at low current densities
- Bottom-up filling as result of accelerator and its by-product accumulation due to rapid decrease in the surface area, especially at the bottom corners of narrow features and suppressor replacement by accelerating species;
- Bump formation & planarization of surface due to replacement of accelerator with leveler and suppressor.

The copper electroplating solution for deep via-filling application can be either Copper sulfate or cyanide-based. Typical composition of an electrolyte includes CuSO₄, H₂SO₄, Cl⁻, additives including Suppressor (Carrier), Accelerator

(Brightener) and Leveler. The electroplating system used for via filling is a research system from Rena. The standard plating solution used is Everplate-Cu200 bought from Atotech. The electroplating process uses pulsed reverse plating which uses 2-component additive system consisting of brightener +leveler.

Copper CMP and wafer back-grind

After the copper via-filling, the over-plated copper is removed by chemical mechanical polishing. In a normal silicon carrier process, further metallization layers are processed before attaching a temporary handle wafer on the front-side and then doing a back-grind and polishing to expose the through silicon copper vias. A wet polishing is an standard process after back-grinding to remove any defects generated due to back-grinding. The same tool has been used for chemical mechanical polishing (CMP) with suitable high etch rate slurry. It may be noted that an appropriate de-ionized water cleaning step is done to remove the slurry residue. A soft-bond back-grinding wheel was used for back-grinding Copper and Silicon together to expose the through silicon vias. A rough grind was first performed to remove major part of the silicon. Then soft grinding wheel was used to expose the copper vias.

The completed silicon carrier wafer is then assembled on a printed wiring board with solder bumps and tested for electrical continuity and via resistance. The carriers were tested for thermal cycle reliability condition -40°C to 125 upto 1000 cycles. The via electrical resistance was monitored as part of the daisy chain connecting chip1, chip 2 & chip 3 to the PCB. The via resistance did not change and cross section showed no failure in the via.

Chain resistance	At T=0 (Ω)	250 cycles (Ω)	500 cycles (Ω)	750 cycles (Ω)	1000 cycles (Ω)
Chip 1 to board	23.9	23.9	24.3	24.3	24.3
Chip 2 to board	21.3	21.5	21.9	22.3	22.3
Chip 3 to board	25.2	25.5	25.9	25.9	26.0

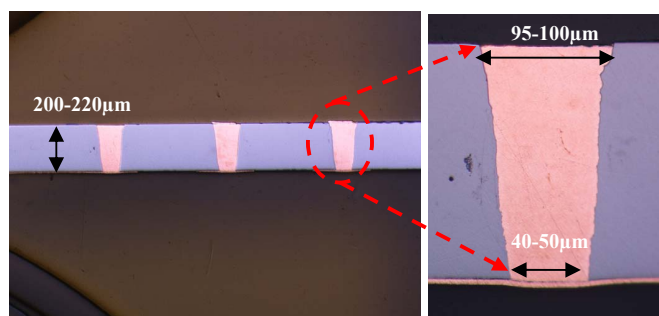


Figure-9: Optical image of cross-sectioned silicon carrier wafer showing a void-free electroplated copper vias. The silicon carrier wafer was back grinded and polished to expose the copper vias on both sides.

Table-5: Process Parameter for Via Exposure by Back-grinding and polishing:

Process Conditions	Rough Grind	Via exposure
Spindle Speed	3200 rpm	2800 rpm
C.T Speed	250 rpm	150 rpm
Cutting depth	400 micron	100 micron
Feed rates	100um/mins	20um/mins
Mesh Sizes	325 #	600 #

Results and Discussion

Figure 4(a) shows that the profile is vertical but sidewalls have the scallops which are typical of BOSCH etch process due to its cyclical nature. After applying via tapering etch process, the profile is modified into a tapered profile as shown in Figure 4(b & c). The results thus show that a vertical etch profile can be tapered and also smoothen the scallops caused by the BOSCH process. It may however be noted that the sidewall roughness due to BOSCH process is < 200nm whereas the sidewall curvature due to second etch step is 5-6μm which is more severe. Thus the third process step has to work harder to remove the curvature and round-off the top corner. This has the effect of increasing the top dimension of the via by 8-10μm due to isotropic nature of the process. It may also be noted that during the via tapering process in step-3 the exposed silicon surface becomes slightly rough. From the surface roughness data in table-3 it can be seen that the recipe#1 has the maximum via tapering effect and also minimum surface roughness of 0.585nm. Hence, this process condition has been finally implemented for carrier fabrication.

The plot in figure 6 shows the dependence of slope of various via geometries on the global isotropic etch process conditions. It can be seen that via tapering effect is higher for vias diameters less than 50μm. It is also seen that via tapering is higher when SF6 is increased and when Argon ions are added to plasma. Hence, from the above data it may be concluded that the most desirable via tapering process should have higher pressure, high SF6 concentration and Argon content. However, based on the surface roughness studies done on different isotropic etch process conditions, it can be seen that recipe-id: #1 causes minimum surface damage while the Argon addition causes maximum surface damage due to higher impact caused on the silicon surface. For the recipe conditions with higher Pressure and higher SF6 concentration as in recipe-ids #2 and #3, the surface roughness is slightly higher than for recipe-d #1. The higher chemical reactivity due to higher pressure and higher SF6 concentration is believed to be the main cause for slight increase in the surface roughness.

Figures 7 and 8 shows the low-temperature PECVD silicon dioxide deposition process characteristics across the wafer and it can be seen that deposition process uniformity close to 5% can be achieved. It is further seen that the process ensures sufficient deposition of dielectric in the sidewall to provide a good electrical isolation.

From figures 8 and 9 we can see that very good void-free copper via filling is achievable by reverse pulse electroplating process in Rena system. It can also be seen that a good

defect free copper CMP and wafer back-grinding process could be achieved in the fabrication of silicon carrier wafers.

Conclusion

Through this work it has been shown that deep silicon vias formed by BOSCH etch process can be tapered by tailoring additional via tapering etch processes and achieve high degree of process control and flexibility by independently controlling each stage of the process. It was shown that a low-temperature dielectric deposition process can be developed which meets the electrical isolation requirements of through silicon electrical interconnects. It was also shown that it is possible to realize a void-free deep silicon copper via-filling by using reverse pulsed copper plating process. The results presented thus meets a critical requirement for forming through-silicon copper interconnection for 3D system in packaging application. It was successfully shown in this work that a high aspect ratio tapered via with aspect ratio of >3 can be achieved by a void-free copper electroplating process. The through silicon via structures were finally qualified after wafer thinning and subjecting them to thermo-mechanical reliability test (-40 to 125°C) and electrical continuity test.

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