SPICE compatible modelling of on-chip coupled interconnects

R. Kumar, K. Kang, S.C. Rustagi, K. Mouthaan and T.K.S. Wong

On-chip coupled interconnect lines are modelled using measured S-parameters. The physical consistency between single and coupled line model parameters are maintained in the proposed methodology. The SPICE compatible model is validated in both the frequency and the time domain using copper and ultra low-κ coupled interconnects.

Introduction: Interconnects play an increasingly dominant role in determining the electrical performance of silicon-based integrated circuits (ICs). The modelling of interconnects is particularly challenging as interconnect models have to accurately account for the lossy nature of the silicon substrate. Coupled lines have been analysed in the literature [1–3]; however, there are limited reports on SPICE compatible coupled line models accounting for the effect of proximity as well as substrate loss. Further, the interconnects with copper and low dielectric constant (κ) materials are currently being used for fabrication of high-performance ICs to reduce RC delay and crosstalk. Ultra-low-κ (ULK) dielectrics with $\kappa \leq 2.2$ are expected to be in use by the year 2009 as per the International Technology Roadmap (2006 update). In this Letter, a measurement-based approach for modelling the frequency and time domain behaviour of single and coupled on-chip interconnects is proposed. Coupled copper interconnect test structures with both undpoped silicon glass (USG) and ULK dielectrics are modelled.

Test structure fabrication and measurements: Single and coupled copper interconnects with widths of 0.15, 0.25, 0.50 and 1 µm, thickness of 0.23 µm, and length of 500 µm were fabricated on a film stack consisting of 10 µm-thick USG and 0.05 µm of SiC deposited on a 200 mm-diameter, <100> oriented p-Si substrate with resistivity of ~10 Ω cm. The metal lines were embedded in a porous methylsilsesquioxane (P-MSQ) dielectric ($\kappa \sim 2.2$) with SiC as etch stop layer for chemical mechanical planarisation (CMP) followed by deposition of 0.05 µm-thick silicon nitride and 0.3 µm-thick USG as passivation layers. A set of test structures with USG as intra-metal dielectrics was also fabricated. The test structures were designed in ground–signal–ground configuration. A transmission electron microscope (TEM) cross-section of the 0.15 µm coupled lines test structure with ULK as dielectric is shown in Fig. 1. The schematic top view of test structure is shown in the inset to Fig.1. The line-to-line spacing between the coupled lines was varied between 1, 3 and 7 times of the respective line widths.

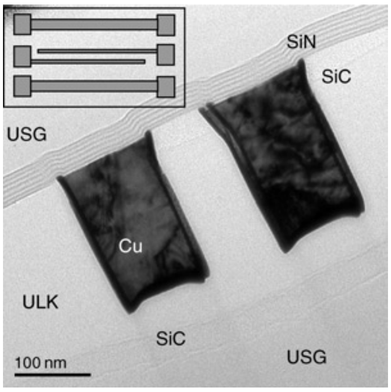

Fig. 1 *TEM cross-section of coupling test structure*

Inset: Schematic top view

On-wafer S-parameter measurements were carried out using Cascade Microtech Infinity probes and an HP8510C network analyser, calibrated using line-reflect-reflect-match (LRRM) technique over a frequency range from 50 MHz to 40 GHz. The measured data was de-embedded using open-dummy pad admittances. The time-domain characterisation was carried out using an Agilent 81134A 3.35 GHz pulse generator and Agilent DSO81204A 12 GHz oscilloscope. Agilent's integrated circuit characterisation and analysis program (IC-CAP) was used in conjunction with SPICE 3 for modelling and simulations.

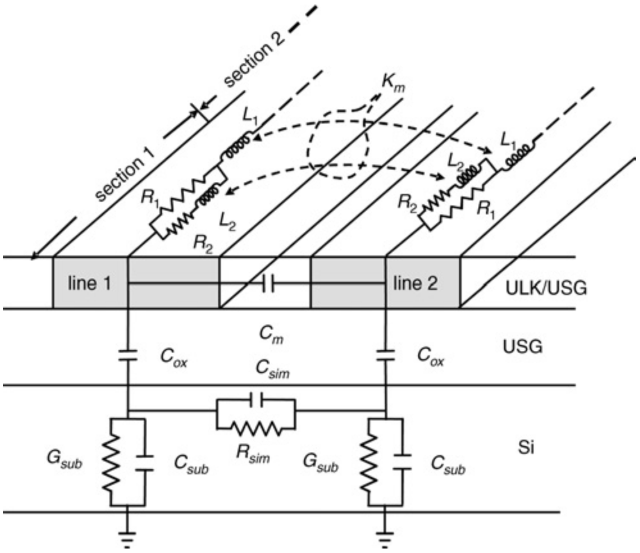

Fig. 2 *Coupled line model consisting of multiple cascaded Γ-sections of single line pairs*

Coupled line models: The coupled line model comprises models of two single lines and the coupling elements, as shown in Fig. 2. For extraction of model parameters for coupled lines, the 500 µm-long, single interconnect lines were modelled first using three cascaded Γ sections of a wideband representation consisting of R_1, R_2, L_1, L_2, C_{ox}, C_{sub} and G_{sub} [4]. The single line model parameters derived from the asymptotic technique [4] were further refined using optimisation routines to improve the accuracy of the extracted parameters for subsequent use in the coupled line model. The match between modelled and measured S-parameters was excellent as RMS errors in the magnitude and phase of the modelled data were below 1.8% for all test structures over a frequency range of 50 MHz to 40 GHz.

In the next step, the model parameters representing the coupling between the two lines were extracted. C_m represents the capacitive coupling between the two interconnect lines and the coefficient of mutual inductance K_m, accounts for the inductive coupling. C_{sim} and G_{sim} account for the electrical coupling and loss through silicon substrate between coupled lines. The initial values of frequency independent coupling parameters were calculated using closed-form expressions available in the literature [5–7]. We also included C_{ox} and R_1 obtained from the single line model during the coupled line parameter optimisation as these two parameters are strongly influenced by proximity effects. All other single line parameters retained their values obtained from the single line model. This maintains the consistency between the single and coupled lines models while taking into account the proximity effects. The extracted values of single line parameters R_2, L_1, L_2, C_{sub} and G_{sub}, which were retained during optimisation of 0.15 µm-wide coupled lines with 0.15 µm spacing, were 1.34 k Ω, 166.5 pH, 0.76 nH, 11.92 fF and 0.68 mS, respectively. The extracted values of R_1, C_{ox}, C_m, K_m, C_{sim} and G_{sim} were found to be 96.5 Ω, 4.64 pF, 19.66 pF, 0.001, 11.5 fF and 1.13 mS, respectively.

Results: Fig. 3 shows the measured and modelled forward transmission S-parameter S_{21} for 0.15 µm-wide coupled lines with line-to-line spacing of 0.15, 0.45 and 1.05 µm, respectively. Excellent agreement between measured and modelled S-parameters is observed. The worst-case RMS error is less than 3.28% for all test structures with line length of 500 µm. The time domain characterisation shown in Fig. 4 shows a good match between the measured and modelled far-end crosstalk signals for a pulse input of 1 V with pulse width of 5 ns, period of 10 ns and a rise/fall time of ~65 ps. The modelled and measured values of crosstalk for coupled lines were compared for another test structure with USG dielectric, which also showed a close match, as shown in Fig. 4. The smaller crosstalk with ULK is on account of reduction in metal thickness as well as the dielectric constant of ULK.

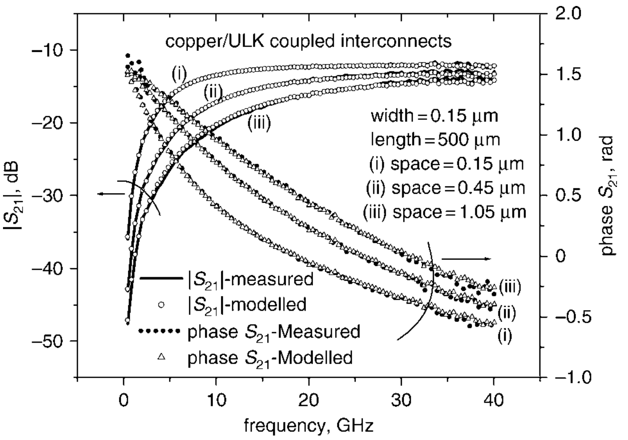

Fig. 3 *Modelled and measured magnitude and phase of S_{21} for coupled interconnects with ULK dielectric*

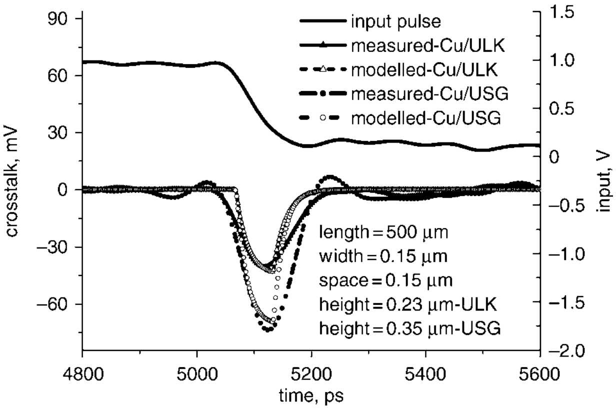

Fig. 4 *Modelled and measured magnitude of crosstalk for coupled interconnects with USG and ULK dielectrics*

Conclusion: A measurement-based methodology is proposed for SPICE compatible modelling of on-chip coupled interconnects. Excellent agreement between the measured and modelled frequency and time domain responses over a wide frequency band up to 40 GHz is obtained.

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