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Strained n-Channel Transistors With Silicon Source and Drain Regions and Embedded Silicon/Germanium as Strain-Transfer Structure

Kah-Wee Ang, Chih-Hang Tung, N. Balasubramanian, Ganesh S. Samudra, and Yee-Chia Yeo

***Abstract*—We report the demonstration of 55 nm gate length L_G strained n-channel field-effect transistors (n-FETs) having an embedded $Si_{1-x}Ge_x$ structure that is beneath the Si channel region and which acts as a strain-transfer structure (STS). The $Si_{1-x}Ge_x$ STS has lattice interactions with both the silicon source and drain regions and with the overlying Si channel region. This effectively results in a transfer of lateral tensile strain to the Si channel region for electron mobility enhancement. The mechanism of strain transfer is explained. Significant drive current I_{on} enhancement of 18% at a fixed off-state leakage I_{off} of 100 nA/μm is achieved, which is attributed to the strain-induced mobility enhancement. Furthermore, continuous downsizing of transistors leads to higher I_{on} enhancement in the strained n-FETs, which is consistent with the increasing transconductance G_m improvement when the gate length is reduced.**

***Index Terms*—Electron mobility, silicon/germanium, strained n-channel field-effect transistor (n-FET), strain-transfer structure (STS).**

I. INTRODUCTION

IN addition to the miniaturization of the MOSFET, further improvement in device performance is achievable by enhancing the carrier transport properties of silicon (Si). Carrier mobility in Si can be improved by strain-induced modification of the electronic band structure. In n-channel MOSFETs, electron mobility is enhanced by using a biaxial tensile strained Si channel formed on a relaxed silicon/germanium ($Si_{1-x}Ge_x$) virtual substrate [1]–[3], or by employing a high-stress silicon nitride (SiN) liner, which mechanically couples the uniaxial tensile stress to the channel region [4]–[7]. In addition, the use of silicon–carbon ($Si_{1-y}C_y$) as source and drain (S/D) stressors also enhances the electron mobility significantly [8], [9]. Recently, strained n-channel field-effect transistor (n-FET) with a $Si_{1-x}Ge_x$ strain-inducing layer embedded beneath the transistor channel was proposed [10], [11]. Device demonstration was only recently reported [12]. The channel strain in this structure is influenced by the thickness t_{Si} of the Si channel, as well as the lateral dimension d_{SiGe} of the SiGe strain-transfer structure (STS) and its thickness t_{SiGe} (see Fig. 1). Channel strain is increased by scaling these structural parameters, i.e., reducing t_{Si} and d_{SiGe}, and increasing t_{SiGe}. In this letter, we investigate further enhancements in an n-FET with embedded $Si_{1-x}Ge_x$ STS, scaling down the lateral dimension d_{SiGe} of the STS as well as the strained Si channel thickness t_{Si} to increase the strain in the transistor channel. The structural parameters (d_{SiGe} and t_{Si}) adopted here are also the smallest realized in such a device structure and would allow the achievement of a higher performance enhancement [12]. Unlike conventional methods of strain introduction, this approach makes use of the lattice interactions at the vertical heterojunction between the Si S/D regions and the embedded $Si_{1-x}Ge_x$ stressor to impart lateral tension in the transistor channel. We also investigate the impact of the strain effects on drive current I_{on} and transconductance G_m enhancement for devices with various gate lengths L_G.

II. DEVICE DESIGN AND FABRICATION

Fig. 1(a) illustrates the lattice interactions in the strained n-FET with an embedded $Si_{1-x}Ge_x$ STS and Si S/D regions. In this device structure, an embedded $Si_{1-x}Ge_x$ stressor is used as a medium to impart tensile strain into the Si channel. At the vertical heterojunction between the embedded $Si_{1-x}Ge_x$ structure and the Si source or drain region, lattice interactions cause a vertical compression of the $Si_{1-x}Ge_x$ lattice. This results in a reduced lateral compression in the $Si_{1-x}Ge_x$ lattice as compared to its as-grown fully strained state. As a consequence of the lattice mismatch, a lateral tension is imparted to the overlying Si channel region, which will be exploited for the enhancement of electron mobility.

The strained n-FETs used in this study were fabricated using a process sequence similar to that described in [9]. After local oxidation of silicon formation, a compressively strained $Si_{1-x}Ge_x$ of 35 nm is selectively grown on the active region followed by the selective epitaxy of a Si capping layer of ~20 nm. The thickness of the $Si_{1-x}Ge_x$ STS is 10 nm thinner than that reported in [12], which could increase the throughput of the epitaxy process. The Ge concentration x in the embedded $Si_{1-x}Ge_x$ STS is 25%. Following gate stack and spacer formation, S/D recess etch was performed. Selective epitaxial growth of Si in the S/D regions was then performed, and a standard

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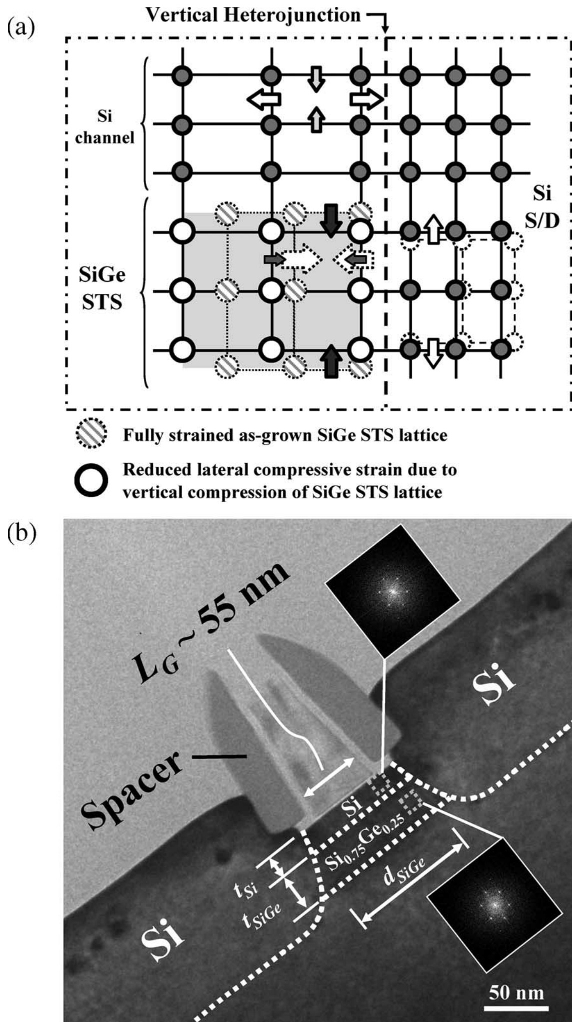


Fig. 1. (a) Schematic illustrating the lattice interactions at the vertical heterojunction between the Si S/D region and the $Si_{1-x}Ge_x$ STS. The Si S/D region compresses the embedded $Si_{1-x}Ge_x$ structure vertically, which results in a reduced lateral compression in the $Si_{1-x}Ge_x$ lattice. This leads to an effective transfer of a lateral tensile strain to the overlying Si channel region. (b) TEM micrograph of a 55-nm gate length L_G strained n-FET featuring an intermediary STS and Si S/D regions. Diffractograms of the Si channel and the embedded $Si_{1-x}Ge_x$ structure reveal excellent crystalline quality, as shown in the inset.

n-channel MOSFET (NMOS) process flow was employed to complete the device fabrication. Fig. 1(b) shows the cross-sectional transmission electron microscopy (TEM) micrograph of a completed strained transistor with Si S/D regions and an embedded $Si_{1-x}Ge_x$ intermediary STS. No misfit dislocations were observed near the vertical heterojunction, indicating a pseudomorphic growth of Si in the S/D regions despite a substantial lattice mismatch with the $Si_{1-x}Ge_x$ region. Diffractograms obtained at the Si channel and embedded $Si_{1-x}Ge_x$ layer reveal excellent crystalline quality [inset of Fig. 1(b)].

III. Results and Discussion

Fig. 2(a) plots the I_{DS}–V_{GS} characteristics of a strained transistor with $Si_{1-x}Ge_x$ STS and a control transistor with raised Si S/D. Similar drain-induced barrier lowering (DIBL) and subthreshold swing are observed for both devices, indicating no adverse effects due to the channel strain engineering. The slightly lower threshold voltage V_{Tsat} observed in the strained device could be attributed to the band offsets induced by strain effects. Fig. 2(b) plots the I_{DS}–V_{DS} characteristics of the control and strained n-FETs with a gate length of 55 nm at various gate overdrives $V_{GS} - V_{Tsat}$. The drive current performance of the strained n-FET is significantly enhanced over the control n-FET when compared at the same gate overdrive $V_{GS} - V_{Tsat}$ of 1.2 V. It should be noted that the drive current performance reported in this letter is not comparable with that reported in the industry [2]–[7] due to the use of a thick gate dielectric thickness (EOT $\approx$ 2.5 nm) and non-silicided S/D regions.

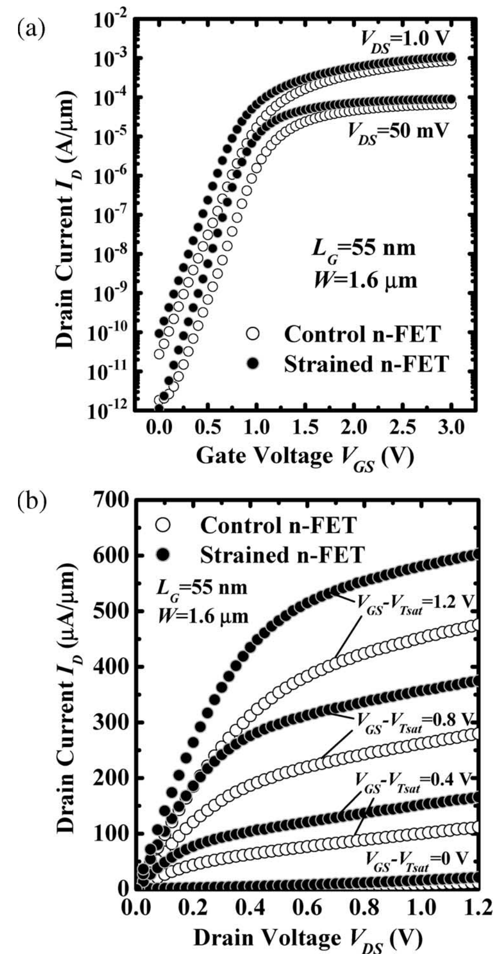


Fig. 2. (a) I_{DS}–V_{GS} characteristics for a pair of closely matched control transistor and strained transistor with a $Si_{0.75}Ge_{0.25}$ STS, showing comparable off-state leakage I_{off}, subthreshold swing, and DIBL. (b) I_{DS}–V_{DS} characteristics show significant drain current enhancement in the strained n-FET over the control n-FET at a gate overdrive $V_{GS} - V_{Tsat}$ of 1.2 V.

Fig. 3(a) examines the enhancement in the saturation drive current I_{on} and the linear transconductance G_{mlin} for the strained devices as compared to the unstrained control devices at various gate lengths. Increasing improvement in I_{on} is achieved with decreasing gate length. This is due to the increased strain effects in short channel devices. For a 55 nm L_G strained transistor, a significant enhancement in maximum G_{mlin} of 48% is observed over the control transistor. In general, higher G_{mlin} gain is achieved when the gate length is reduced. A comparison of the saturation drive current I_{on} at a fixed

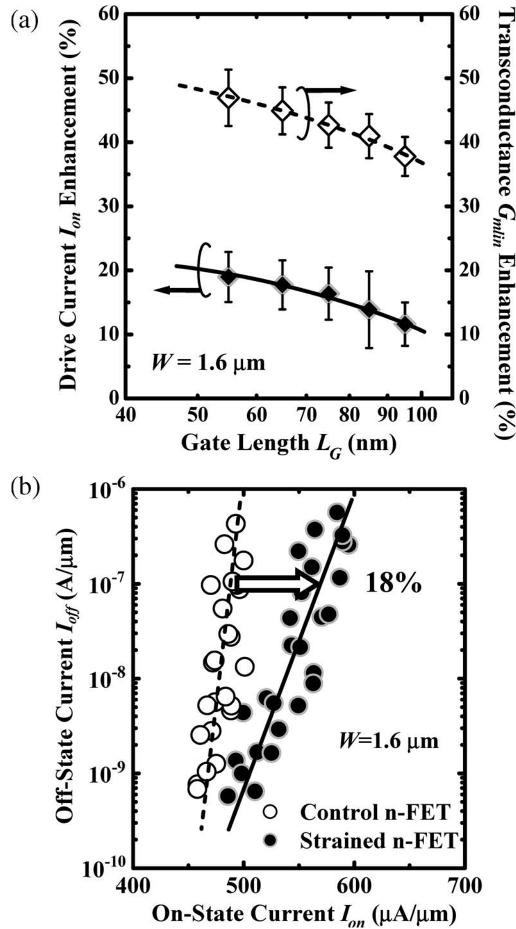
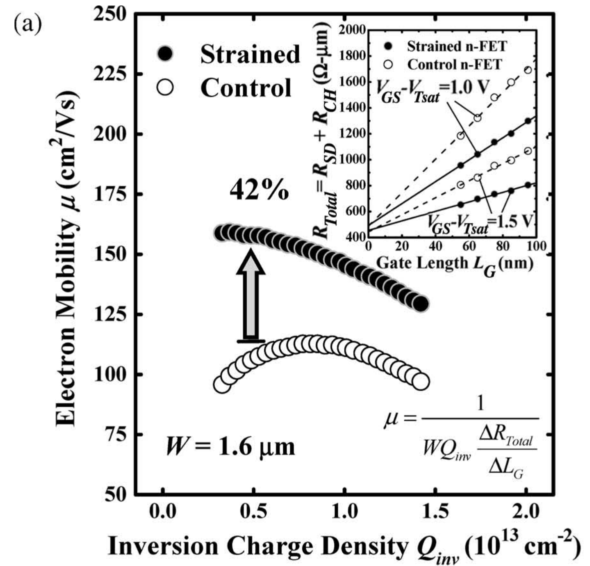


Fig. 3. (a) Enhancement of the saturation drive current $I_{\rm on}$ and the linear transconductance $G_{\rm mlin}$ in the strained devices as a function of gate length L_G. Higher $I_{\rm on}$ and $G_{\rm mlin}$ improvements are observed at smaller L_G, illustrating the increasing benefits of strain-induced effects with device scaling. (b) At an off-state leakage $I_{\rm off}$ of 100 nA/μm, strained n-FETs show 18% $I_{\rm on}$ enhancement over the control n-FETs. The $I_{\rm on}$ is measured at $V_{\rm GS} - V_{\rm Tsat} = 1.2$ V and $V_{\rm DS} = 1.0$ V, whereas the $I_{\rm off}$ is measured at $V_{\rm GS} = V_{\rm Tsat} - 0.2$ V and $V_{\rm DS} = 1.0$ V.



(b)

Strain Engineering Approaches	Mobility Gain (%)	I_{on} Gain (%)	I_{Dlin} Gain (%)
SiN tensile liner [14]	27	11	2
Stress Memorization [14]	35	10	11
$Si_{1-y}C_y$ S/D stressors [15]	70	35	55
Reverse embedded SiGe [12]	39	15	-
n-FET with SiGe strain transfer structure [this work]	**42**	**18**	**36**

Fig. 4. (a) Strained n-FET demonstrates significant mobility enhancement of ~42% over the unstrained control n-FET, which is attributed to the beneficial tensile strain induced in the transistor channel. (b) Table summarizes the mobility, saturation drive current $I_{\rm on}$, and linear drive current $I_{\rm Dlin}$ improvements offered by the various strain engineering approaches for n-FETs.

off-state leakage $I_{\rm off}$ between control and strained devices is depicted in Fig. 3(b). The $I_{\rm on}$ is measured at $V_{\rm GS} - V_{\rm Tsat} = 1.2$ V and $V_{\rm DS} = 1.0$ V, whereas the $I_{\rm off}$ is measured at $V_{\rm GS} = V_{\rm Tsat} - 0.2$ V and $V_{\rm DS} = 1.0$ V. At an $I_{\rm off}$ of 100 nA/μm, the strained devices show an $I_{\rm on}$ enhancement of 18% over the control devices, which is predominantly attributed to strain effects. This improvement is observed to be higher than that reported in a strained n-FET with reverse embedded SiGe structure due to increased strain level in the transistor channel when the structural parameters are scaled down [12]. Stress calculation using 2-D finite-element simulator shows that an average stress level of ~750 MPa is induced at the top 5 nm of the Si channel region for a transistor with geometrical features resembling that fabricated in this letter [Fig. 1(b)].

Fig. 4(a) plots the electron mobility as a function of inversion charge density for both control and strained transistors. The effective electron mobility was extracted based on a total resistance slope-based approach reported in [13]. Note that this approach eliminates the series resistance effects. It was observed that strained transistors demonstrate a significant mobility enhancement of ~42% over the unstrained control transistors. The inset of Fig. 4(a) depicts that the series resistances of both devices are comparable due to similar raised Si S/D regions, illustrating that the observed mobility enhancement is predominantly due to strain-induced effects. Strain lifts the six-fold degeneracy of the conduction bands and leads to carrier transport mass reduction, which concomitantly results in enhanced electron mobility [9]. This mobility improvement is higher than the typical mobility gain reported for n-FETs with high-stress silicon nitride liner or stress memorization technique [14]. Fig. 4(b) shows a summary of mobility, saturation drive current $I_{\rm on}$, and linear drive current $I_{\rm Dlin}$ improvements in n-FETs offered by the various strain engineering approaches reported-to-date. Strained n-FETs with an intermediary STS is a promising option for extending the carrier mobility and drive current performance of future high-speed devices as it utilizes more mature SiGe and Si epitaxy technology.

IV. Conclusion

A novel 55 nm gate length strained n-FET with a $Si_{1-x}Ge_x$ STS and Si S/D regions was demonstrated. Through lattice interactions between the Si S/D region and the embedded $Si_{1-x}Ge_x$ structure, lateral tensile strain can be imparted into the transistor channel. Significant mobility gain of $\sim$42% and saturation drive current I_{on} enhancement of 18% were achieved with this transistor structure. In addition, further scaling of transistors leads to larger I_{on} enhancement, making this a promising strain engineering scheme for future technology generations.

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