Copyright © 2007 Year IEEE. Reprinted from IEEE ELECTRON DEVICE LETTERS, VOL. 28, NO. 11, NOVEMBER 2007. Such permission of the IEEE does not in any way imply IEEE endorsement of any of Institute of Microelectronics' products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permission@ieee.org.

N-Channel (110)-Sidewall Strained FinFETs With Silicon–Carbon Source and Drain Stressors and Tensile Capping Layer

Tsung-Yang Liow, Kian-Ming Tan, Rinus T. P. Lee, Chih-Hang Tung, Ganesh S. Samudra, N. Balasubramanian, and Yee-Chia Yeo

***Abstract*—The performance of n-channel (110)-sidewall trigate fin-shaped field-effect transistors (FinFETs) is seriously compromised as (110) surfaces have significantly lower electron mobility than (100) surfaces. Straining the channel in (110)-sidewall FinFETs using lattice-mismatched silicon–carbon ($Si_{1-y}C_y$) stressors alone was experimentally determined to be far less effective than doing the same with (100)-sidewall FinFETs. By additionally incorporating a tensile silicon nitride contact etch-stop layer, the increase in longitudinal tensile stress and the introduction of vertical compressive stress result in significant further I_{Dsat} enhancement, highlighting the importance of the vertical compressive stress component for enhancing (110)-sidewall FinFET performance.**

***Index Terms*—Etch-stop layer (ESL), fin-shaped field-effect transistor (FinFET), multiple-gate transistor, silicon–carbon (SiC), strain, stress.**

I. Introduction

TRANSISTORS with a multiple-gate structure, such as fin-shaped field-effect transistors (FinFETs), can be scaled well beyond the 32-nm technology node [1]–[3]. The sidewall channel surface orientation of a FinFET depends on its channel direction. To maximize n- and p-channel FinFET drive currents, fins with (100) and (110) sidewalls, respectively, should be ideally used [4]. However, this also incurs an area penalty, which is undesirable in density-critical applications such as static random access memory [5]. This area penalty can be avoided by using fins with (110) sidewalls for n- and p-channel FinFETs, which then compromises the performance of n-channel FinFETs due to drastically lower electron mobility on (110) surfaces. This makes the use of mobility-enhancement techniques such as strain engineering very important for n-channel (110)-sidewall FinFETs.

Manuscript received July 9, 2007; revised August 6, 2007. This work was supported by a research grant from Nanoelectronics Research Program, Agency for Science, Technology and Research, Singapore (A*STAR). The review of this letter was arranged by Editor M. Ostling.

T.-Y. Liow is with Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119260, and also with the Institute of Microelectronics, Singapore 117685.

K.-M. Tan, R. T. P. Lee, G. S. Samudra, and Y.-C. Yeo are with Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119260 (e-mail: yeo@ieee.org; eleyeoyc@nus.edu.sg).

C.-H. Tung and N. Balasubramanian are with the Institute of Microelectronics, Singapore 117685.

Digital Object Identifier 10.1109/LED.2007.908495

It has been recently reported how strain engineering can significantly improve electron mobility on (110) surfaces [6]. There also have been previous strain engineering reports on improving n-channel (110)-sidewall FinFET performance, involving the use of strained silicon-on-insulator (sSOI) [7], [8], high stress silicon nitride (SiN) etch-stop layer (ESL) [9]–[11], or a combination of both [12]. Integration of multiple stressors with the inclusion of silicon–carbon ($Si_{1-y}C_y$ or SiC) source and drain (S/D) for (110)-sidewall n-channel FinFETs has never been explored before. Raising the FinFET's S/D regions by selective Si epitaxy is vital for reducing external resistance [13]. By selectively growing lattice-mismatched $Si_{1-y}C_y$ [14] instead of Si, we have previously obtained significant strain-induced I_{Dsat} performance enhancement for (100)-sidewall FinFETs [15]. In this letter, we report the first demonstration of (110)-sidewall FinFETs featuring both $Si_{1-y}C_y$ S/D stressors and a high stress SiN ESL, and the effectiveness of cumulative stress on electrical performance.

II. Device Fabrication

Trigate n-channel FinFETs were fabricated on 50-nm-thick SOI wafers with (001) surface orientation and a buried oxide thickness of 140 nm. For a trigate (110)-sidewall FinFET with a 30-nm-wide fin, 77% of the total channel surface area is of the (110) surface orientation [i.e., $(2 \times H_{\mathrm{Fin}})/(2 \times H_{\mathrm{Fin}} + W_{\mathrm{Fin}})$]. In the absence of strain, the low electron mobility of the (110) sidewalls severely impacts the performance of the trigate (110)-sidewall FinFET. To improve the performance of the (110)-sidewall FinFET, channel stress was induced by $Si_{1-y}C_y$ S/D stressors alone or by the combined use of $Si_{1-y}C_y$ S/D stressors and tensile SiN ESL.

The fabrication process flow is identical to that described in [15]. Fin widths down to ~30 nm were obtained by 248-nm photolithography, photoresist trimming, and etching. The gate stack comprised 2 nm of SiO_2 and 70 nm of polysilicon. The SiN gate spacer formation step involved a further *in situ* etch to remove SiN stringers that would otherwise surround the fin sidewalls. This allows selective epitaxial growth (SEG) of either Si or $Si_{1-y}C_y$ on the top and sidewall surfaces of the S/D regions, reducing parasitic S/D series resistance. For FinFETs with $Si_{1-y}C_y$ S/D stressors, this further enables greater lattice strain coupling to the channel. Fig. 1 shows a structural schematic of the experiment splits. Forty nanometers

0741-3106/$25.00 © 2007 IEEE

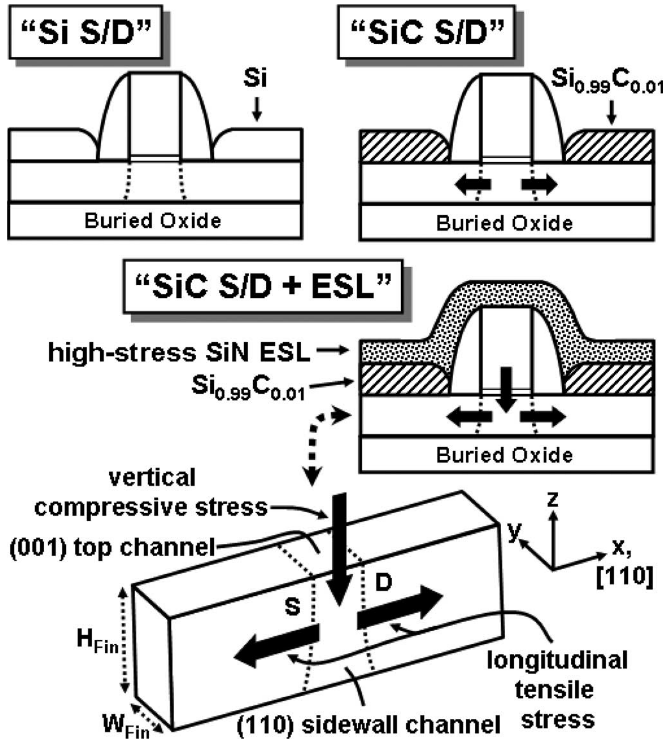

Fig. 1. Schematic showing the three experiment splits or device structures comprising "Si S/D," "SiC S/D," and "SiC S/D+ESL." In the "Si S/D" control split, the devices have raised Si S/D regions. In the "SiC S/D" and "SiC S/D+ESL" splits, the devices have raised $Si_{1-y}C_y$ S/D regions. In the "SiC S/D+ESL" split, an additional tensile SiN ESL was deposited. A 3-D schematic of the fin is also shown for the "SiC S/D+ESL" split, in which the stress components acting on the (110)-sidewall channel surface are also indicated.

of Si was grown selectively in the S/D regions for the "Si S/D" split, which serves as a control. For the "SiC S/D" and "SiC S/D+ESL" splits, the raised S/D comprised 35 nm of $Si_{0.99}C_{0.01}$ (1% substitutional carbon) instead, predominantly inducing uniaxial longitudinal stress in the channel. An additional 40-nm-thick tensile (+1.1 GPa) SiN ESL was deposited for the "SiC S/D+ESL" split, which further increases uniaxial longitudinal stress, as well as vertical compressive stress, in the channel.

A major challenge is the *in situ* native oxide removal in an ultrahigh vacuum (UHV) chemical vapor deposition reactor prior to SEG of SiC. A brief *in situ* anneal at 750–850 °C in UHV ambient is typically used; however, this still causes undesirable agglomeration or migration of Si [16], [17], leading to broken fins in our experiments. We reduced the anneal temperature to 700 °C (for ∼10 s) to resolve the problem. In the future, fins with smaller dimensions are more susceptible to this effect, as the critical temperature for Si agglomeration decreases with decreasing SOI thickness [18]. Epitaxy reactors, which eliminate the need for a UHV anneal, e.g., with an *in situ* chemical-based native oxide removal chamber, would be advantageous.

III. Results and Discussion

Fig. 2 plots the $I_{\rm Off}-I_{\rm On}$ characteristics of (110)-sidewall FinFETs with Si S/D, SiC S/D, and SiC S/D and SiN ESL.

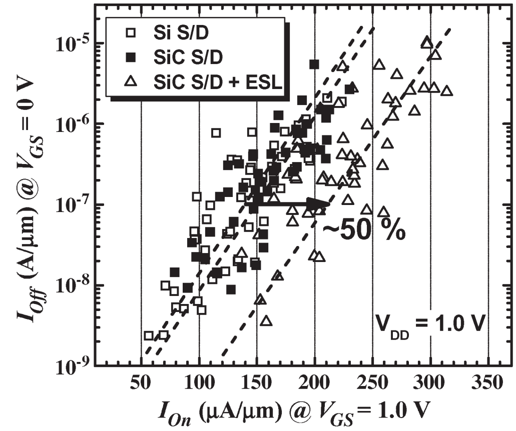

Fig. 2. $I_{\rm Off}-I_{\rm On}$ characteristics of FinFETs with Si S/D, SiC S/D, and SiC S/D and ESL. For (110)-sidewall FinFETs, incorporating $Si_{1-y}C_y$ S/D stressors alone results in a modest performance enhancement. However, further addition of a tensile SiN ESL results in significant performance enhancement.

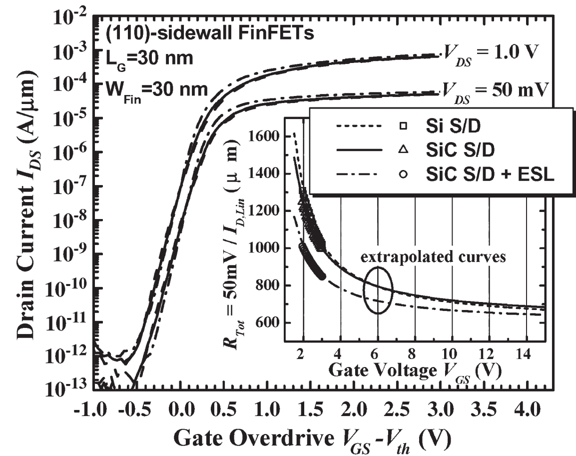

Fig. 3. Subthreshold characteristics of FinFETs with Si S/D, SiC S/D, and SiC S/D and ESL, showing similar values of DIBL and subthreshold slope. The fin sidewall surface is a (110) surface. $I_{\rm DS}$ is plotted against $V_{\rm GS}-V_{\rm th}$ for a clearer illustration, where $V_{\rm th}=V_{\rm GS}$ at $I_{\rm DS}=100$ nA/μm, when $V_{\rm DS}=1.0$ V. The values of $V_{\rm th}$ are 84, 40, and 2 mV for "Si S/D," "SiC S/D," and "SiC S/D+ESL," respectively. The threshold voltage lowering in "SiC S/D" and "SiC S/D+ESL" is attributed to strain-induced conduction band lowering. The inset shows total resistance ($R_{\rm Tot}=50$ mV$/I_{D,\rm lin}$) plotted against gate voltage. A simplified linear region drain current equation that includes an S/D series resistance parameter was used to generate curves that fit each set of measured data points. The series resistance were estimated to be 594, 614, and 595 $\Omega\cdot\mu$m for "Si S/D," "SiC S/D," and "SiC S/D+ESL," respectively. It should be noted that the comparison of selected devices with similar DIBL, subthreshold slope, and series resistance does not give as much statistical information on device performance as the $I_{\rm Off}-I_{\rm On}$ plot (Fig. 2).

Modest $I_{\rm On}$ enhancement resulted from the sole incorporation of $Si_{1-y}C_y$ S/D stressors. By additionally incorporating a tensile ESL stressor in the "SiC S/D+ESL" FinFETs, very significant $I_{\rm On}$ enhancement was observed as a result of combined stress effects from the two stressors. At a given $I_{\rm Off}$ of 100 nA/μm, this enhancement was ∼50% over the control FinFETs with Si S/D. To facilitate closer examination, efforts were made to ensure that FinFETs with similar gate lengths, fin widths, and S/D series resistance were chosen for further analysis. Fig. 3 shows the subthreshold characteristics of (110)-sidewall FinFETs with Si S/D, SiC S/D, and SiC S/D and

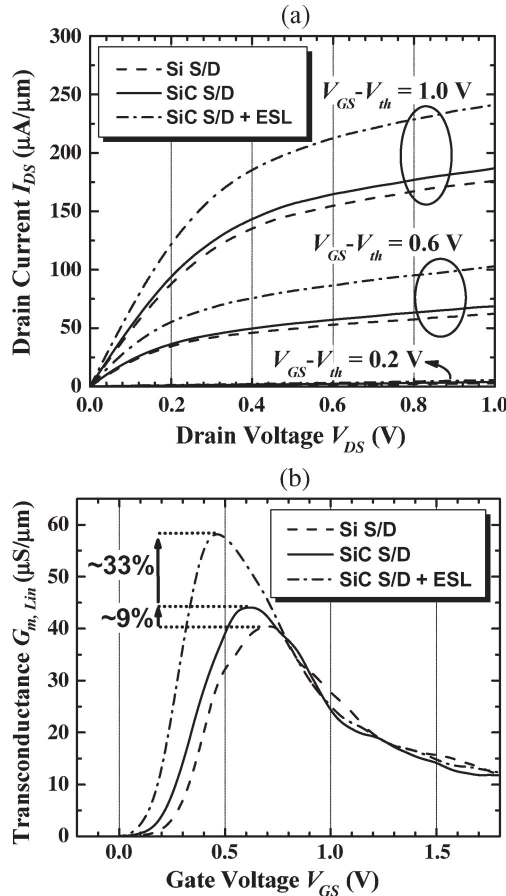

Fig. 4. (a) $I_{\rm DS}$–$V_{\rm DS}$ characteristics of the FinFETs at various gate overdrives, $V_{\rm GS}$–$V_{\rm th}$. $I_{\rm DSat}$ enhancement of about 6% was obtained by incorporating $\mathrm{Si}_{1-y}\mathrm{C}_y$ S/D stressors alone, whereas a further 29% enhancement can be obtained by adding a tensile SiN ESL, bringing the total enhancement to ∼37%. $V_{\rm th}$ is defined as $V_{\rm GS}$ when $I_{\rm DS} = 100$ nA/μm and $V_{\rm DS} = 1.0$ V. (b) $G_{m,\rm Lin}$–$V_{\rm GS}$ characteristics showing the corresponding enhancement in peak linear transconductance, which is attributed to strain-induced mobility enhancement.

SiN ESL. These devices show similar values of drain-induced barrier lowering (DIBL) and subthreshold slope, suggesting that their effective gate lengths and fin widths are comparable. The inset shows a plot of total resistance ($R_{\rm Tot} = 50$ mV$/I_{D,\rm lin}$) against gate voltage. A simplified linear region drain current equation that includes an S/D series resistance fitting parameter was used to fit each set of measured data points, estimating the series resistance to be comparable as well—594, 614, and 595 Ω μm for "Si S/D," "SiC S/D," and "SiC S/D+ESL," respectively. Fig. 4(a) shows the $I_{\rm DS}$–$V_{\rm DS}$ family of curves for those devices. At a gate overdrive $(V_{\rm GS}$–$V_{\rm th})$ of 1.0 V, an $I_{\rm Dsat}$ enhancement of about 6% was obtained by solely incorporating $\mathrm{Si}_{1-y}\mathrm{C}_y$ S/D stressors, which predominantly induces uniaxial longitudinal tensile stress in the channel. Channel stress in nanoscale devices is not easily measurable due to metrological challenges. Peak $G_{m,\rm Lin}$, which is related to mobility, also increases by 9% [Fig. 4(b)]. The $I_{\rm Dsat}$ enhancement for these (110)-sidewall devices with $\mathrm{Si}_{1-y}\mathrm{C}_y$ S/D stressors only is lower than the 20% enhancement that was previously obtained with (100)-sidewall counterparts [15]. However, this is in good agreement with the piezoresistance model [19] if predominantly uniaxial longitudinal stress ($\sigma_{\rm xx}$ much greater than $\sigma_{\rm yy}$ or $\sigma_{\rm zz}$) is assumed. Since the longitudinal piezoresistance coefficient for the channel surfaces in a (110)-sidewall FinFET is only 30.5% that of the channel surfaces in a (100)-sidewall FinFET [19], [20], the sensitivity of the (110)-sidewall FinFET to uniaxial longitudinal stress is also correspondingly lower. Hence, the uniaxial longitudinal tensile stress induced by the $\mathrm{Si}_{1-y}\mathrm{C}_y$ S/D stressors alone may be inadequate for enhancing the performance of the (110)-sidewall FinFET.

By depositing an additional tensile stress ESL, $I_{\rm Dsat}$ performance is further enhanced by 29%, resulting in a significant total enhancement of 37% [Fig. 4(a)]. Correspondingly, a 33% increase in peak $G_{m,\rm Lin}$ is also observed, bringing the total $G_{m,\rm Lin}$ enhancement to 45% over the control device [Fig. 4(b)]. A tensile stress ESL is expected to bring about an increase in longitudinal tensile stress ($\sigma_{\rm xx}$ becomes more tensile) as well as an increase in vertical compressive stress [$\sigma_{\rm zz}$ becomes more compressive (see Fig. 1)] [9]. For the $(110)/\langle 110\rangle$ sidewall channel surfaces, it has been reported that longitudinal tensile stress and vertical compressive stress result in electron mobility enhancement, with vertical compressive stress having a greater effect in the lower stress regime [6]. As such, it is reasonable to believe that vertical compressive stress plays a major role in the mobility enhancement of the $(110)/\langle 110\rangle$ sidewall channel surfaces. It should be noted that a FinFET with Si S/D+ESL stressors would allow the impact of ESL stressor alone to be identified; however, this has been already explored in [9] and [10].

The effect of SiC S/D and SiC S/D+ESL stressors on the performance of n-channel (110)-sidewall trigate FinFETs is summarized in Table I based on the data extracted from $I_{\rm Off}$–$I_{\rm On}$ plots. The data from (100)-sidewall counterparts have been included for comparison. A meaningful comparison can be made despite the relatively low absolute drive currents, which can be attributed to the large equivalent oxide thickness and the high $R_{\rm SD}$ due to the unsilicided S/D regions. It is clear that (100)-sidewall FinFETs with combined SiC S/D and ESL stressors exhibit the best overall $I_{\rm On}$ performance. For (110)-sidewall FinFETs, integration with combined SiC S/D and ESL stressors leads to a 51% $I_{\rm On}$ enhancement, which makes their absolute $I_{\rm On}$ performance superior to that of unstrained Si S/D as well as strained SiC S/D (100)-sidewall counterparts. The enhancement is also larger than that reported in [9] and can be partially due to the higher SiN film stress. In addition, the thinner polysilicon gate and narrower spacers could be also contributing factors for better stress coupling from the ESL stressor to the channel. Further device optimization may involve the adjustment of carbon content in SiC, tensile stress level in SiN, and geometrical parameters such as the spacer width and raised S/D height (which affects channel stress, parasitic capacitance, and series resistance), and could be performed using technology computer-aided design tools.

IV. Conclusion

It is desirable to have longitudinal tensile stress and vertical compressive stress for improving the performance of n-channel

TABLE I
EFFECT OF SiC S/D AND SiC S/D+ESL STRESSORS ON FinFET PERFORMANCE

	(100)-sidewall FinFETs			(110)-sidewall FinFETs		
Device Structure	*Si S/D*	*SiC S/D*	*SiC S/D +ESL*	*Si S/D*	*SiC S/D*	*SiC S/D +ESL*
I_{On} @ I_{Off} = 1 x 10^{-7}A, V_{DD} = 1.0 V (μA/μm)	167	200	261	140	149	211
$\Delta I_{On}/I_{On,\,Si\,S/D}$ (%)	0	20	56	0	6	51

(110)-sidewall FinFETs. A raised S/D architecture is likely to be essential for alleviating parasitic S/D series resistance effects in FinFETs. By adopting lattice-mismatched $Si_{1-y}C_y$ as the raised S/D material for n-channel FinFETs, electron mobility enhancement due to uniaxial longitudinal tensile stress provides an additional performance boost. To further enhance the performance of (110)-sidewall FinFETs with $Si_{1-y}C_y$ S/D stressors, a tensile stress ESL should be added. This induces additional longitudinal tensile stress and, more importantly, a significant amount of vertical compressive stress. The combination of these two types of stressors was experimentally demonstrated to provide a 51% I_{On} enhancement at an I_{Off} of 100 nA/μm in (110)-sidewall trigate well-tempered FinFETs, resulting in absolute performance that surpasses that of unstrained (100)-sidewall counterparts.

ACKNOWLEDGMENT

T.-Y. Liow would like to thank A∗STAR for a Graduate Scholarship Award. K.-M. Tan would also like to thank the National University of Singapore and Chartered Semiconductor Manufacturing, Singapore, for a Graduate Scholarship Award.

REFERENCES

[1] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Andersen, T.-J. King, J. Bokor, and C. Hu, "FinFET—A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320–2325, Dec. 2000.

[2] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King, J. Bokor, C. Hu, M.-R. Lin, and D. Kyser, "FinFET scaling to 10 nm gate length," in *IEDM Tech. Dig.*, 2002, pp. 251–254.

[3] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y.-C. Yeo, Y. Li, J.-W. Lee, P. Chen, M.-S. Liang, and C. Hu, "5 nm-gate nanowire FinFET," in *VLSI Symp. Tech. Dig.*, 2004, pp. 196–197.

[4] L. Chang, Y. K. Choi, D. Ha, P. Ranade, S. Xiong, J. Bokor, C. Hu, and T.-J. King, "Extremely scaled silicon nano-CMOS devices," *Proc. IEEE*, vol. 91, no. 11, pp. 1860–1873, Nov. 2003.

[5] Z. Guo, S. Balasubramanian, R. Ziatanovici, T.-J. King, and B. Nikolic, "FinFET-based SRAM design," in *Proc. ISLPED*, 2005, pp. 2–7.

[6] K. Uchida, A. Kinoshita, and M. Saitoh, "Carrier transport in (110) nMOSFETs: Subband structures, non-parabolicity, mobility characteristics, and uniaxial stress engineering," in *IEDM Tech. Dig.*, 2006, pp. 1–3.

[7] W. Xiong, C. R. Cleavelin, P. Kohli, C. Huffman, T. Schulz, K. Schruefer, G. Gebara, K. Mathews, P. Patruno, Y.-M. Le Vaillant, I. Cayrefourcq, M. Kennard, C. Mazure, K. Shin, and T.-J. K. Liu, "Impact of strained-silicon-on-insulator (sSOI) substrate on FinFET mobility," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1019–1021.

[8] T. Irisawa, T. Numata, T. Tezuka, N. Sugiyama, and S. Takagi, "Electron transport properties of ultrathin-body and tri-gate SOI nMOSFETs with biaxial and uniaxial strain," in *IEDM Tech. Dig.*, 2006, pp. 457–460.

[9] N. Collaert, A. De Keersgieter, K. G. Anil, R. Rooyackers, G. Eneman, M. Goodwin, B. Eyckens, E. Sleeckx, J.-F. de Marneffe, K. De Meyer, P. Absil, M. Jurczak, and S. Biesemans, "Performance improvement of tall triple gate devices with strained SiN layers," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 820–822, Nov. 2005.

[10] K. Shin, C. O. Chui, and T.-J. King, "Dual stress capping layer enhancement study for hybrid orientation FinFET CMOS technology," in *IEDM Tech. Dig.*, 2005, pp. 1009–1012.

[11] J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick, and R. Chau, "Tri-gate transistor architecture with high-k gate dielectrics, metal gates and strain engineering," in *VLSI Symp. Tech. Dig.*, 2006, pp. 62–63.

[12] N. Collaert, R. Rooyackers, F. Clemente, P. Zimmerman, I. Cayrefourcq, B. Ghyselen, K. T. San, B. Eyckens, M. Jurczak, and S. Biesemans, "Performance enhancement of MuGFET devices using super critical strained-SOI (SC-SSOI) and CESL," in *VLSI Symp. Tech. Dig.*, 2006, pp. 64–65.

[13] J. Kedzierski, M. Ieong, E. Nowak, T. S. Kanarsky, Y. Zhang, R. Roy, D. Boyd, D. Fried, and H.-S. P. Wong, "Extension and source/drain design for high-performance FinFET devices," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 952–958, Apr. 2003.

[14] Y.-C. Yeo, "Enhancing CMOS transistor performance using lattice-mismatched materials in source/drain regions," *Semicond. Sci. Technol.*, vol. 22, no. 1, pp. S177–S182, Jan. 2007.

[15] T.-Y. Liow, K.-M. Tan, R. T. P. Lee, A. Du, C.-H. Tung, G. S. Samudra, W.-J. Yoo, N. Balasubramanian, and Y.-C. Yeo, "Strained n-channel FinFETs with 25 nm gate length and silicon–carbon source/drain regions for performance enhancement," in *VLSI Symp. Tech. Dig.*, 2006, pp. 68–69.

[16] Y. Ishikawa, M. Kumezawa, R. Nuryadi, and M. Tabe, "Effect of patterning on thermal agglomeration of ultrathin silicon-on-insulator layer," *Appl. Surf. Sci.*, vol. 190, no. 1, pp. 11–15, May 2002.

[17] Y. Ishikawa, Y. Imai, H. Ikeda, and M. Tabe, "Pattern-induced alignment of silicon islands on buried oxide layer of silicon-on-insulator structure," *Appl. Phys. Lett.*, vol. 83, no. 15, pp. 3162–3164, Oct. 2003.

[18] R. Nuryadi, Y. Ishikawa, Y. Ono, and M. Tabe, "Thermal agglomeration of single-crystalline Si layer on buried SiO_2 in ultrahigh vacuum," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 20, no. 1, pp. 167–172, Jan./Feb. 2002.

[19] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Phys. Rev.*, vol. 94, no. 1, pp. 42–49, Apr. 1954.

[20] Y. Kanda, "A graphical representation of the piezoresistance coefficients in silicon," *IEEE Trans. Electron Devices*, vol. ED-29, no. 1, pp. 64–70, Jan. 1982.