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# Low-Temperature Transport Characteristics and Quantum-Confinement Effects in Gate-All-Around Si-Nanowire N-MOSFET

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**Abstract**—Gate-all-around n-MOSFETs with Si-nanowire ( $\sim 7$  nm) as the channel body are fabricated and characterized for their low-temperature behavior ( $\sim 5$  K to 295 K).  $I_{DS}$ - $V_{GS}$  characteristics at low  $V_{DS}$  ( $\sim 50$  mV) exhibit a decrease in current with decreasing temperature in strong inversion up to about  $\sim 200$  K. However, at high  $V_{DS}$ , drain current reverts to typical temperature behavior, i.e.,  $I_{DS}$  increases with the reducing temperature due to the increase in phonon-limited mobility ( $\mu_{ph}$ ). It is inferred that, at low  $V_{DS}$ , the enhancement in  $\mu_{ph}$  at a reduced temperature could be possibly masked by the intersubband scattering on account of subband splitting due to quantum-confinement effects as indicated by subband calculations for nanowire structures.

**Index Terms**—Carrier transport, gate all around, low temperature, MOSFET, silicon nanowire (SiNW).

## I. INTRODUCTION

SILICON nanowires (SiNWs) are attractive for many nanoelectronic applications, including those as channel bodies in field-effect-transistors (FETs) [1]–[5]. Several approaches including bottom-up approaches [6]–[8] and top-down approaches [2]–[4], [9] have been reported for realization of nanowire-based devices. As these nonplanar device architectures tend to emerge for CMOS and other novel applications, comprehensive assessment of carrier transport mechanisms assumes importance. These devices provide a unique opportunity to probe the quantum mechanical effects on carrier transport in low dimensions. Oscillations in  $I_{DS}$  and mobility at very low  $V_{DS}$  (0.2 mV) and low temperature for trigated FETs with fin width  $\times$  height  $\sim 45 \times 82$  nm<sup>2</sup> have been reported [10], [11].

This letter reports the low-temperature device behavior of  $\sim 7$ -nm-thick SiNW channel MOSFETs with fully surrounding poly-Si gates prepared by a top-down approach. Devices are characterized in the temperature range of 5 K–295 K, and effects of subband splitting are evidenced even at higher gate and drain bias levels and higher temperature than hitherto reported. Inferences are drawn with the help of simple subband calculations based on the solution of Schrödinger's equation and effective mass density of states (DOS) in the subbands.

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## II. DEVICE FABRICATION AND CHARACTERIZATION

Starting with 8" (100) SOI substrate with top Si (p-type,  $\sim 10^{15}$  cm<sup>-3</sup>) thickness of  $\sim 200$  nm, Si-fins of width  $\sim 40$ – $50$  nm with different lengths (300–1000 nm, and results for 300 nm are reported in this letter) were patterned and etched down to buried oxide. The wafers were then oxidized in dry O<sub>2</sub> at 875 °C for 4 h, resulting in two Si-cores (wires) [4], [9]—one at the bottom and the other close to the top of the fin. The top wire was removed during dry etch (C<sub>4</sub>F<sub>8</sub>) of oxide over source/drain (S/D) areas, and bottom wire was released from the oxide by wet etch in 1:25 diluted hydrofluoric acid. The wafers were oxidized to grow 4-nm-thick SiO<sub>2</sub> as gate dielectric in dry O<sub>2</sub> at 800 °C. It was followed by deposition of  $\sim 130$  nm  $\alpha$ -Si and by gate pattern transfer, As-implant ( $4 \times 10^{15}$  cm<sup>-2</sup>/30 keV) doping of S/D and  $\alpha$ -Si gate, dopant activation (950 °C/15 min), standard metal contact formation, and sintering.

For low-temperature characterization, the devices were bonded onto a thermally conductive ceramic chip carrier which was then plugged into a holder that was lowered into a He-cooled Janis Research cryostat that can cool down to  $\sim 4$  K. Lakeshore-340 temperature controller was used to stabilize the temperature at various chosen values. HP 4156A parameter analyzer was used for all dc characterizations.

## III. RESULTS AND DISCUSSION

At room temperature, the devices have high normalized ON-current ( $I_{DS}$  at  $V_{DS} = V_{GS} = 1.2$  V) of  $\sim 0.68$  mA/ $\mu$ m (normalized to wire thickness of  $\sim 7$  nm, as shown in the inset of Fig. 1),  $V_{TH} \sim 0.2$  V, and subthreshold swing (SS) of  $\sim 68$  mV/dec. Low drain-induced barrier lowering (DIBL) of  $\sim 10$  mV/V is obtained, with  $I_{ON}/I_{OFF} > 10^5$  and low gate leakage of  $\sim 2$ – $5$  pA at room temperature. These results are similar to those reported on nanowire omega-gated FETs by Yang *et al.* [2] (e.g., body of  $\sim 10$  nm, SS of  $\sim 75$  mV/dec, and DIBL of  $\sim 80$  mV/V) and more recently by Suk *et al.* [3] on  $\sim 10$ -nm twin wires (e.g.,  $\sim 70$  mV/dec and  $\sim 20$  mV/V).

When the temperature is reduced, interesting results are observed. Fig. 1(a) shows the measured  $I_{DS}$ - $V_{GS}$  characteristics with  $V_{DS} = 50$  mV at different temperatures in both linear and log scales to delineate the subthreshold and strong inversion regions. Similar to the low-temperature effect in bulk devices in the subthreshold region [12],  $I_{DS}$  reduces as temperature decreases on account of increase in  $V_{TH}$ . However, even in

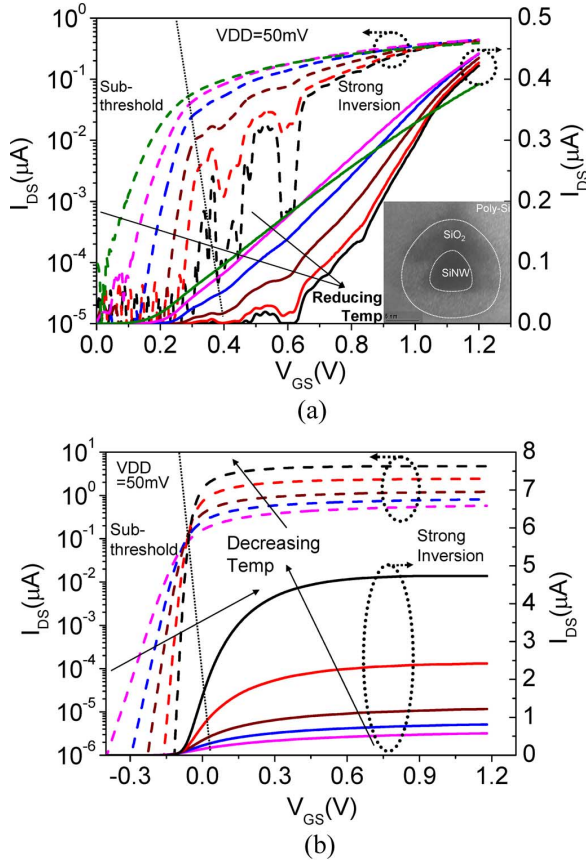


Fig. 1. (a) Measured  $I_{DS}$ - $V_{GS}$  characteristics of  $\sim 7$ -nm triangular SiNW n-FET with effective gate length of  $\sim 300$  nm at different temperatures (5 K, 37 K, 77 K, 137 K, 200 K, and 295 K) at  $V_{DS} = 50$  mV. (b) Simulated  $I_{DS}$ - $V_{GS}$  characteristics of the nanowire n-FET at different temperatures using MEDICI for cylindrical cross section for a 300-nm-long device with 7-nm diameter at 40 K, 77 K, 137 K, 200 K, and 295 K. The inset shows the TEM micrograph of the nanowire channel cross section along with gate oxide.

the strong inversion, the current remains lower at lower temperatures than that at higher temperature, as can be seen from the linear scale. This is contrary to the intuitive expectation, since the increase in mobility ( $\mu_{ph}$ ) from reduced phonon scattering would be expected to enhance the current at lower temperatures which is supported by MEDICI computation of the  $I_{DS}$ - $V_{GS}$  characteristics at  $V_{DS} = 50$  mV using cylindrical coordinates [13] shown in Fig. 1(b). Modified local DOS model for inversion channel, Lombardi's mobility model, and incomplete ionization to account for carrier freeze-out have been used. These simulated characteristics show a behavior similar to that of bulk MOSFET. Subband splitting is not captured in MEDICI simulations, and therefore, we speculate that, in strong inversion, the measured lower values of the linear region current at low temperatures in nanowire MOSFET are due to intersubband scattering on account of quantum-confinement effects.

To explore the quantum-confinement effects, we consider the Schrödinger's equation in cylindrical coordinates [14].

$$-\frac{\hbar^2}{8\pi^2 m^*} \left( \frac{\partial^2 \psi(r)}{\partial r^2} + r \frac{\partial \psi(r)}{\partial r} - \frac{m^2 \psi(r)}{r^2} \right) = (E - V(r)) \psi(r) \quad (1)$$

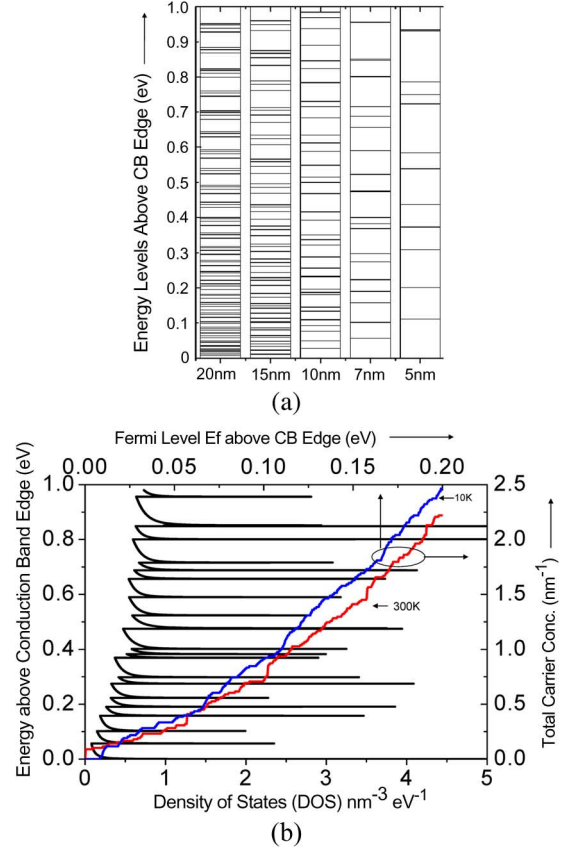


Fig. 2. (a) Discrete energy levels for different diameters of the nanowire from solution of Schrödinger's equation. (b) Effective mass DOS in the nanowire with 7-nm diameter. The total carrier concentration as obtained from the integration of the product of Fermi-Dirac distribution function and DOS as a function of Fermi level is also plotted at 10 K and 300 K.

where “ $m$ ” is the angular quantization index arising due to cylindrical symmetry. Equation (1) has a solution in terms of Bessel's function of the first kind with energy Eigenvalues given by

$$E_{m,n} = \frac{\hbar^2}{8\pi m^* r_0^2} \lambda_{m,n}^2 \quad (2)$$

Here,  $\lambda_{m,n}$  is the  $n^{\text{th}}$  root of  $m^{\text{th}}$ -order Bessel's function. Fig. 2(a) shows the discrete energy levels  $E_{m,n}$  for different diameters of the nanowires, clearly showing the increase in separation of energy levels with decrease in the diameter. We observe that the discrete energy levels differ by as much as 50 meV for a nanowire of  $\sim 7$ -nm diameter. Similar results are reported in [15]–[17].

Furthermore, we calculated the total carrier charge in channel per unit length as

$$n = \int_{E_c}^{\infty} D(E) f(E) dE \quad (3)$$

where  $f(E)$  is the well-known Fermi–Dirac distribution function, and  $D(E)$  is the effective mass DOS given by

$$D(E) = \frac{1}{\pi A_{nw}} \sqrt{\frac{2m^*}{\hbar^2}} \sqrt{\frac{1}{E - E_{m,n}}}. \quad (4)$$

For  $\sim 7$ -nm-thick nanowires, we have chosen  $0.2m_0$  as the effective mass [18], [19] for DOS calculations, where  $m_0$  is the rest mass of electron. The DOS and total charge per unit length are plotted in Fig. 2(b). We plot the carrier charge as a function of Fermi level, the range of which is decided by  $V_{GS}$  as we did not solve the Poisson’s equation simultaneously with Schrödinger’s equation. Such an approach is frequently used in calculating the gate charge in carbon-nanotube FET devices [20]. Interestingly, the total carrier charge increases monotonically with the Fermi level at all temperatures. This implies that the appearance of the valleys in the drain current with increasing gate bias at 5 K and 37 K is mainly due to nonavailability of allowed states for the carriers to participate in current conduction until the next subband is brought within the thermal energy vicinity at that temperature. In other words, the intersubband scattering [10] is very strong at these temperatures. While the valleys in the drain current disappear at temperature beyond 77 K, the magnitude of the current increases with temperature up to 200 K. This can be ascribed to the reduction in intersubband scattering with increasing temperature. The decrease in current with further increase in temperature to 295 K is due to the diminished value of phonon-limited mobility  $\mu_{ph}$ . Thus, the impact of the intersubband scattering vis-à-vis  $\mu_{ph}$  becomes less significant as the temperature increases. It may be worthwhile to note here that, due to smaller separation between the energy eigenvalues when the channel cross sections are wider ( $\sim 0.15$  meV for  $45 \text{ nm} \times 82 \text{ nm}$  [10]), the intersubband scattering may not be as significant.

When we plot the total carrier concentration in the cross-section of the nanowire as a function of  $E_F$ , the data seem to vary in somewhat steplike manner due to the fact that the effective mass DOS increases steeply as the energy level approaches  $E_{m,n}$  eigenvalue. The self-consistent solutions at room temperature [15]–[17], however, do not show such behavior, as the total charge in the nanowire is expected to vary smoothly with increasing gate voltage. The carriers are able to occupy higher subbands due to higher values of thermal energy which broadens the tail in the Fermi-distribution function.

As  $V_{DS}$  increases, the drain current reverts back to the behavior similar to that of bulk MOSFETs—the lower the temperature, the higher the  $I_{DS}$ , as shown in Fig. 3. The reduced impact of the intersubband scattering at higher drain voltages can be understood by the fact that the electron quasi-Fermi level in the channel changes at the rates of  $\sim 160 \mu\text{V}/\text{nm}$  and  $\sim 4 \text{ mV}/\text{nm}$  at  $V_{DS} = 50 \text{ mV}$  and  $V_{DS} = 1.2 \text{ V}$ , respectively. As the higher subbands come in spatial vicinity due to the fast spatial variation of electron quasi-Fermi levels, the effect of the intersubband scattering is reduced at higher  $V_{DS}$ , leading to a qualitatively bulk-type low-temperature behavior. These investigations indicate that the effect of the intersubband scattering can be paramount, particularly at low  $V_{DS}$  and low temperature,

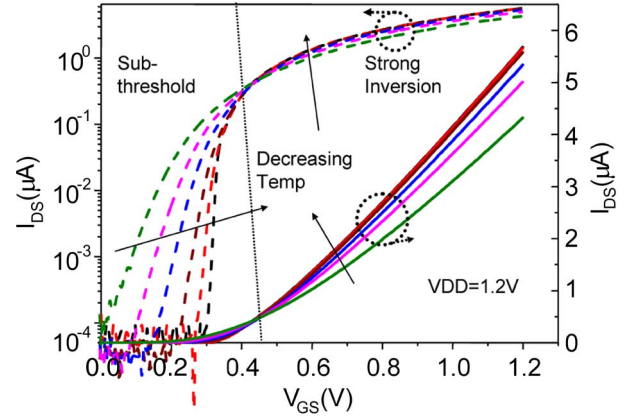


Fig. 3. Measured  $I_{DS}$ – $V_{GS}$  characteristics of  $\sim 7$ -nm triangular SiNW n-FET with effective gate length of  $\sim 300$  nm at different temperatures at  $V_{DS} = 1.2 \text{ V}$  at 5 K, 37 K, 77 K, 137 K, 200 K, and 295 K.

and should be considered up-front in the analysis, e.g., for model development.

#### IV. CONCLUSION

This letter reported the impact of low temperature on carrier–transport behavior, along with the discussion of quantum-confinement effects, for GAA n-MOSFETs with  $\sim 7$ -nm wire channel.  $I_{DS}$  in strong inversion region at low  $V_{DS}$  ( $\leq 50 \text{ mV}$ ) was found to decrease with decreasing temperature, whereas at higher  $V_{DS}$  (e.g.,  $1.2 \text{ V}$ ),  $I_{DS}$  increased with reducing temperature. The effect of enhancement of mobility with decreasing temperature at low  $V_{DS}$  is observable only down to 200 K. This has been speculated to be caused by the quantum-confinement effects leading to subband splitting, giving rise to a strong intersubband scattering which, however, diminishes at higher  $V_{DS}$ .

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#### REFERENCES

- [1] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, “High performance silicon nanowire field effect transistors,” *Nano Lett.*, vol. 3, no. 2, pp. 149–152, 2003.
- [2] F. L. Yang, D. H. Lee, H. Y. Chen, C. Y. Chang, S. D. Liu, C. C. Huang, T. X. Chung, H. W. Chen, C. C. Huang, Y. H. Liu, C. C. Wu, C. C. Chen, S. C. Chen, Y. T. Chen, Y. H. Chen, C. J. Chen, B. W. Chan, P. F. Hsu, J. H. Shieh, H. J. Tao, Y. C. Yeo, Y. Li, J. W. Lee, P. Chen, M. S. Liang, and C. Hu, “5 nm-gate nanowire FinFET,” in *VLSI Symp. Tech. Dig.*, 2004, pp. 196–197.
- [3] S. D. Suk, S. Y. Lee, S. M. Kim, E. J. Yoon, M. S. Kim, M. Li, C. W. Oh, K. H. Yeo, S. H. Kim, D. S. Shin, K. H. Lee, H. S. Park, J. N. Han, C. J. Park, J. B. Park, D. W. Kim, D. Park, and B. I. Ryu, “High performance 5 nm radius twin silicon nanowire MOSFET (TSNWFET): Fabrication on bulk Si wafer, characteristics, and reliability,” in *IEDM Tech. Dig.*, 2005, pp. 735–738.
- [4] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D.-L. Kwong,

- "High-performance fully depleted silicon nanowire (diameter  $\leq 5$  nm) gate-all-around CMOS devices," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 383–386, May 2006.
- [5] Y. Huang, X. Duan, Y. Cui, L. J. Lauhon, K. H. Kim, and C. M. Lieber, "Logic gates and computation from assembled nanowire building blocks," *Science*, vol. 294, no. 5545, pp. 1313–1317, Nov. 2001.
- [6] Y. Cui, L. J. Lauhon, M. S. Gudixsen, J. Wang, and C. M. Lieber, "Diameter-controlled synthesis of single-crystal silicon nanowires," *Appl. Phys. Lett.*, vol. 78, no. 15, pp. 2214–2216, Apr. 2001.
- [7] T. I. Kamins, R. S. Williams, Y. Chen, Y. L. Chang, and Y. A. Chang, "Chemical vapor deposition of Si nanowires nucleated by  $\text{TiSi}_2$  islands on Si," *Appl. Phys. Lett.*, vol. 76, no. 5, pp. 562–564, Jan. 2000.
- [8] D. D. D. Ma, C. S. Lee, F. C. K. Au, S. Y. Tong, and S. T. Lee, "Small-diameter silicon nanowire surfaces," *Science*, vol. 299, no. 5614, pp. 1874–1877, Mar. 2003.
- [9] J. Kedzierski, J. Bokor, and C. Kisielowski, "Fabrication of planar silicon nanowire on silicon-on-insulator using stress limited oxidation," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 15, no. 6, pp. 2825–2828, Nov./Dec. 1997.
- [10] J. P. Colinge, A. J. Quinn, L. Floyd, G. Redmond, J. C. Alderman, W. Xiong, C. R. Cleavelin, T. Schulz, K. Schroefer, G. Knoblinger, and P. Patruno, "Low-temperature electron mobility in trigate SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 27, no. 2, pp. 120–122, Feb. 2006.
- [11] J. P. Colinge, L. Floyd, A. J. Quinn, G. Redmond, J. C. Alderman, W. Xiong, C. R. Cleavelin, T. Schulz, K. Schroefer, G. Knoblinger, and P. Patruno, "Temperature effects on trigate SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 27, no. 3, pp. 172–174, Mar. 2006.
- [12] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 1998, pp. 224–231.
- [13] J. A. Kenrow, "Characterization and analysis of OFET devices based on TCAD simulations," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 2035–2041, Sep. 2005.
- [14] X. Zhou, S. A. Dayeh, D. Aplin, D. Wang, and E. T. Yu, "Scanned electrical probe characterization of carrier transport behaviour in InAs nanowires," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 24, no. 4, pp. 2036–2040, Jul./Aug. 2006.
- [15] A. Marchi, E. Gnani, S. Reggiani, M. Rudan, and G. Baccarani, "Investigating the performance limits silicon nanowires and carbon-nanotube FETs," *Solid State Electron.*, vol. 50, no. 1, pp. 78–85, Jan. 2006.
- [16] E. Gnani, A. Marchi, S. Reggiani, M. Rudan, and G. Baccarani, "Quantum-mechanical analysis of the electrostatics in silicon-nanowire and carbon-nanotube FETs," *Solid State Electron.*, vol. 50, no. 4, pp. 709–715, Apr. 2006.
- [17] J. P. Colinge, J. C. Alderman, W. Xiong, and C. R. Cleavelin, "Quantum-mechanical effects in trigate SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1131–1136, May 2006.
- [18] K. Nehari, N. Cavassilas, J. L. Autran, M. Bescond, D. Munteanu, and M. Lannoo, "Influence of band structure on electron ballistic transport in silicon nanowire MOSFETs: An atomistic study," *Solid State Electron.*, vol. 50, no. 4, pp. 716–721, Apr. 2006.
- [19] J. Wang, A. Rahman, G. Klimeck, and M. Lundstrom, "Band structure and orientation effects in ballistic Si and Ge nanowire FETs," in *IEDM Tech. Dig.*, 2005, pp. 537–540.
- [20] J. O'Keeffe, "Bandstructure modulation for carbon nanotubes in a uniform electric field," *Appl. Phys. Lett.*, vol. 80, no. 4, pp. 676–678, Jan. 2002.