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Flicker Noise and Its Degradation Characteristics Under Electrical Stress in MOSFETs With Thin Strained-Si/SiGe Dual-Quantum Well

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Abstract—This letter reports on the low-frequency flicker-noise characteristics in fresh and electrically stressed pMOSFETs with thin strained-Si (~ 4 nm)/Si_{0.6}Ge_{0.4} (~ 4 nm) dual-quantum-well (DQW) channel architectures. Normalized power spectral density (NPSD) of I_d fluctuations (S_{ID}/I_d^2) in fresh DQW devices exhibits significant improvement (by $> 10^2 \times$) due to buried channel operation at low V_g . At high V_g , the NPSD enhancement reduces as carriers populate in the parasitic surface channel. Upon electrical stress, noise behavior in DQW devices was found to evolve from being carrier number-fluctuation dominated to mobility-fluctuation dominated. This was accompanied by the observation of a “less-distinct” buried-channel operation, indicating a potential stability issue of the Si/SiGe structure.

Index Terms—Electrical stress, flicker noise, interface traps, Si/SiGe dual-quantum well (DQW).

I. INTRODUCTION

CHANNEL architectures incorporating multiple SiGe quantum wells have been studied, showing promising performance improvement when adopted in both PMOS and NMOS short channel transistors, due to increased channel electron and hole mobility [1]. At the same time, local layer strain relaxation is avoided [1], [2]. Meanwhile, better noise performance for Si/Si_{1-x}Ge_x pMOSFETs has been reported by several groups [3]–[8]. Carrier number-fluctuation [4], [6], [7] and/or mobility-fluctuation [3] models were used to analyze the noise performance improvements in such devices. A possible cause for the improvement could be the attenuating effect from Si-capping layer, which can mainly be attributed to the physical separation of holes from the SiO₂/Si interface and its confinement within the buried SiGe channel. Changes in low-frequency noise characteristics with Fowler–Nordheim (F–N) stress have previously been studied in Si_{0.8}Ge_{0.2} pMOSFETs with different Si-capping layer thicknesses [8]. The dual-quantum well (DQW) structure adopted in this letter features SiGe layers with 40% Ge concentration, resulting in larger valence band offset, and hence more pronounced buried channel operation. Furthermore, the low-frequency noise characteristics and degradation mechanisms of DQW devices under electrical

stress have never been reported. Based on the evolution of low-frequency noise behavior at various gate overdrive voltages with electrical stress, the degradation mechanisms for DQW devices are also discussed in this letter.

II. DEVICE FABRICATION AND MEASUREMENT

In this experiment, p-type Si wafers with (001) surface orientation were used. N-well was formed by phosphorous implants at 70 keV followed by 1000 °C/20 s activation in N₂ ambient. After standard RCA cleaning, undoped Si (~ 4 nm)/Si_{0.6}Ge_{0.4} (~ 4 nm) epitaxial layers were grown on Si substrate at 530 °C for two cycles in a cold wall ultrahigh vacuum chemical vapor deposition system to form the DQW channel (total ~ 16 nm). In the control Si device, this epitaxy step was skipped. The DQW structure was chosen for its excellent thermal stability [1], [9]. High-resolution transmission electron microscopy (HRTEM) showed sharp heterointerface transitions between Si and SiGe layers. Using an HRTEM lattice strain analysis method [10], strains in the surface and buried Si layers were determined to be tensile, i.e., +0.7% and +1.0%, respectively. The buried SiGe layers were compressively strained, i.e., –0.6% for the layer nearer to the surface and –1.3% for the layer farther away from the surface. The rms surface roughness of the epi stack was ~ 0.09 nm as measured by atomic force microscope, which is comparable to that of the starting Si surface. After channel formation, LP-TEOS SiO₂ with a thickness of 10 nm was deposited as gate oxide at 650 °C, followed by 130-nm poly-Si deposition (550 °C) and BF₃⁺ implantation. After gate patterning, BF₃⁺ implantation and 1000 °C spike annealing were performed for source/drain formation, followed by standard metallization scheme for contact formation and forming gas anneal at 420 °C. Noise measurements on pMOSFETs with gate length of 0.5 μ m were performed at room temperature using Keithley model 428 low-noise preamplifier and HP35670A Dynamic Signal Analyzer for frequency spectrum measurement. DC electrical characterization and electrical stressing was performed using HP4156C parameter analyzer.

III. RESULTS AND DISCUSSION

Due to the use of strained-Si and SiGe channels, a very large enhancement in drive current was generally observed in all devices. Fig. 1 compares the g_m characteristics of the DQW Si_{0.6}Ge_{0.4} device and the control silicon device. DQW device exhibits two distinct g_m peaks. The first peak corresponds

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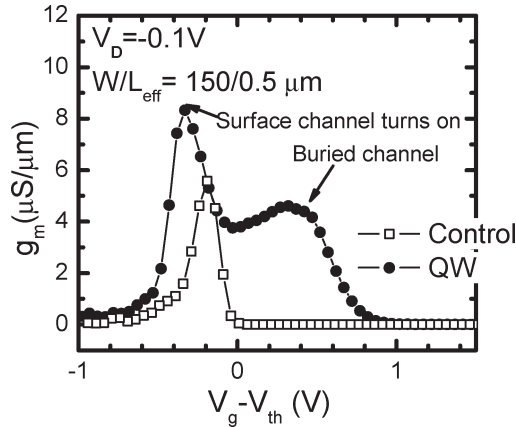


Fig. 1. Transconductance g_m versus $V_g - V_{th}$ characteristics for both (solid) DQW and (open) conventional silicon control MOSFETs.

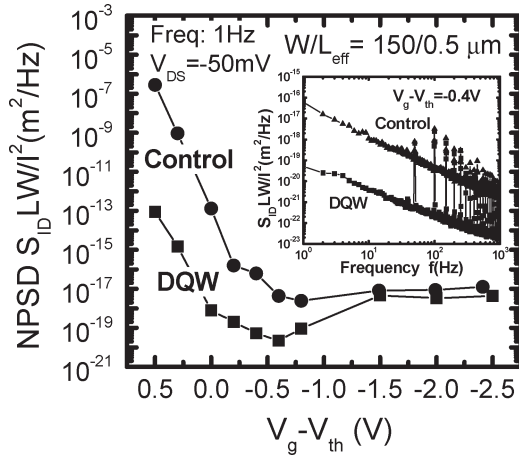


Fig. 2. NPSD versus $V_g - V_{th}$ characteristics at 1 Hz of DQW and silicon control MOSFETs. NPSD versus frequency is shown as inset.

to the onset of buried channel inversion, whereas the second peak (at a higher gate overdrive) corresponds to the onset of surface channel inversion. The magnitude of the second peak is probably larger due to contributions from both the surface and buried channels. The rapid decrease of g_m when at high gate overdrive voltages suggests that the source and drain resistances may have nonnegligible contributions to the measured noise at high gate overdrive voltages.

Fig. 2 compares the NPSD of I_d fluctuations ($S_{ID}LW/I_d^2$) as function of $V_g - V_{th}$ for DQW and Si-control devices. For the frequency range of 1–1600 Hz, the flicker noise of the DQW device is $\sim 10^2 \times$ lower than that of the control device at low gate bias (i.e., $|V_g - V_{th}| < 0.5$ V). This is consistent with previous reports [3] and is attributed to the preferential population of holes in the buried SiGe quantum wells. With increasing gate bias, NPSD in both the control and DQW devices decreased. In the DQW device, holes begin to populate the parasitic Si surface channel at high gate bias. This parasitic conduction layer behaves like the conventional Si surface device, resulting in a noise spectral density that approaches that of the Si control device. Therefore, the noise behavior in DQW devices is dependent upon the gate bias condition, which determines the carrier distribution. At even higher gate bias, the

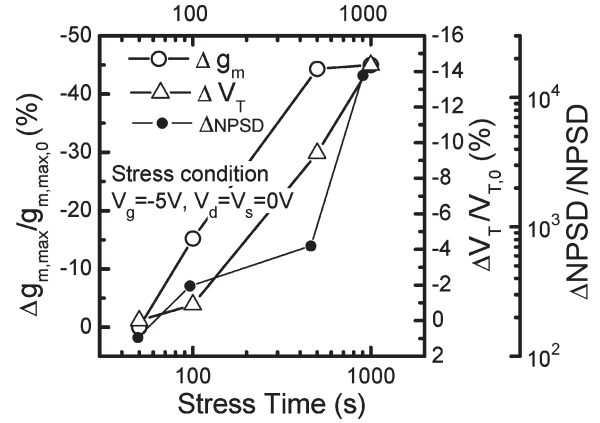


Fig. 3. Relative change in g_m , V_T , and NPSD (measured at $V_g - V_T = -0.8$ V) with stress time.

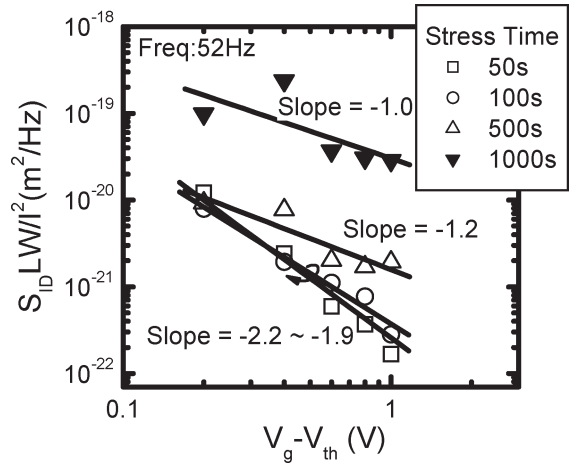


Fig. 4. NPSD (at 52 Hz) of the DQW pMOSFET versus $V_g - V_{th}$ after stressing the gate with a constant voltage of -5 V for durations of 50, 100, 500, and 1000 s. Gradients extracted from linear fits of the data points indicate a shift in noise behavior from carrier number-fluctuation dominated to carrier mobility-fluctuation dominated.

contribution of noise from the source and drain resistors also become nonnegligible, and could also be partially responsible for the reduction in noise performance enhancement.

Device degradation was characterized based on F–N stress. Constant voltage stress was applied at $V_g = -5$ V with grounded source and drain. Fig. 3 summarizes the evolution of major device parameters (ΔV_T , Δg_m , ΔS_{ID}) with stress time. Normalized S_{ID} was measured in the strong inversion regime ($V_{ds} = -50$ mV, $V_g - V_T = -0.8$ V). The shift in V_T is probably caused by hole trapping in the gate oxide. The degradation in S_{ID} with electrical stress is attributed to the generation of oxide traps and interface states and can also be due to the increase in proportion of surface conduction. Interestingly, we also observed that the g_m peak corresponding to the buried-channel disappeared quickly upon electrical stressing, whereas the g_m peak corresponding to the onset of surface channel conduction persisted. Thus, $g_{m,max}$ shown in Fig. 3 is the maximum of the peak corresponding to the onset of surface channel conduction. The g_m peak was significantly degraded with electrical stress, suggesting correspondingly significant degradation in mobility.

Fig. 4 plots NPSD of a DQW device against gate bias ($V_g - V_{th}$) for various durations of stress, showing the evolution of NPSD-gate bias characteristics with electrical stressing. With short stress times, it can be seen that S_{ID}/I_d^2 versus $V_g - V_{th}$ exhibits a slope of -2 which agrees with the formalism of the carrier number-fluctuation model (Δn) for low V_{ds} conditions, when plotted in the log-log scale (inset). Our results show differences compared with previous results obtained in $\text{Si}_{0.7}\text{Ge}_{0.3}$ pMOSFETs by von Haartman *et al.* [3], who reported a mobility-fluctuation-dominated mechanism. They investigated and attributed this to a surface roughness scattering process. On the other hand, our results concur with [6]–[8], who report similar carrier number-fluctuation dominance. As such, it seems possible that buried channel pMOSFETs can show carrier mobility-fluctuation-dominated or carrier number-fluctuation-dominated noise behavior. The cause of this discrepancy can possibly be due to differences in channel architecture, Si/SiGe epitaxial processes, Ge concentration, and thermal processes.

After 500 s of electrical stress, S_{ID}/I_d^2 becomes proportional to $(V_g - V_{th})^{-1}$. This is in agreement with the carrier mobility-fluctuation ($\Delta\mu$) model adopted in [3], indicating the change in noise behavior to one that is dominated by carrier mobility fluctuation. A clue for this change in noise behavior can be found in [3], in which von Haartman *et al.* reported a mobility fluctuation noise behavior in their pMOSFETs that is more pronounced in surface channel Si devices than in buried channel SiGe devices. This, together with the disappearance of the g_m peak corresponding to the onset of buried channel inversion upon electrical stressing, suggests an increased higher proportion of surface conduction with prolonged electrical stressing. This apparent shift toward surface conduction is hard to explain, but can perhaps be attributed to rapid degradation of the Si/SiGe interface with electrical stressing.

IV. CONCLUSION

Strained-Si/SiGe DQW pMOSFETs show nearly $\sim 10^2$ to 10^3 lower flicker-noise levels compared to control Si devices. However, DQW devices degrade quickly under F–N stress,

both in mobility as well as noise performance. With prolonged stress, the noise behavior evolves from being dominated by carrier number fluctuation to carrier mobility fluctuation. The results seem to point toward rapid degradation of the Si/SiGe interface and an increase in surface conduction under prolonged electrical stress. Although SiGe QW devices bring about large performance benefits, it may be necessary to extensively evaluate their electrical stress stability.

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