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Reduced carrier backscattering in heterojunction SiGe nanowire channels

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In this work, we investigate the effect of energy band profile modulation on carrier backscattering in SiGe nanowire (SGNW) heterojunction *p*-channel field effect transistors. The energy band profile is modulated by increasing the Ge mole fraction in nanowire channels as compared to source/drain regions using the pattern-dependent Ge condensation technique. The carrier backscattering characteristics of the fabricated heterojunction *p*-type SGNW transistors, extracted using a temperature-dependent analytical model, exhibited a decrease of 19% in hole backscattering coefficient in comparison to the reference planar devices with uniform Ge concentration. The reduction in backscattering coefficient is attributed to KT/q barrier layer thinning of the source-to-channel barrier for the holes as a result of the modulation in energy band profile caused by variation in Ge concentration. © 2008 American Institute of Physics. [DOI: 10.1063/1.3050527]

Field effect transistors (FETs) employing silicon nanowires (NWs) as the channel body are being presented as promising candidates for future high performance logic requirements.^{1,2} Superior short channel immunity and quasi-ballistic carrier transport make such extremely scaled FETs very attractive.^{3–5} Ge (Ref. 6) or SiGe (Ref. 7) NW FETs are expected to perform even better as both the electrons and holes exhibit higher intrinsic mobility in germanium than in silicon. Engineering the energy band profile in the transistor's source, channel, and drain regions can result in improved carrier transport.⁸ Intuitively, combining the energy band profile engineering with a Ge-enriched Si NW channel can exploit both advantages; however, its physical realization is nontrivial.

Ge condensation is a phenomenon that occurs in SiGe alloys during thermal oxidation. Under the right conditions, it is possible to selectively oxidize Si, while Ge atoms are rejected from the oxidation front.⁹ This effectively enriches the SiGe alloy with Ge during oxidation. By applying the Ge condensation technique on patterned SiGe structures, a lateral heterostructure can be formed depending on the pattern shape. This was used to fabricate SiGe NW (SGNW) FETs with Ge concentration modulation from source/drain (S/D) (30%) to channel (70%). In this letter, the effects of the modified energy band profile as a result of Ge concentration variation in these heterojunction SiGe NW FETs are discussed alongside comparisons with planar homojunction SiGe devices. Using a temperature-dependent channel backscattering analytical model,¹⁰ the backscattering characteristic of the SiGe NW devices was investigated. A decrease of 19% in backscattering coefficient was achieved in the SiGe NW heterostructure compared with the homojunction device, which also suggests a large enhancement in hole injection efficiency in such lateral heterojunction SGNW devices. Reduction in backscattering coefficient is attributed to the decrease in KT/q hole barrier layer thickness as a result of the

valence band offset between the source and the channel regions.

In this work, *p*-type ($1 \times 10^{15} \text{ cm}^{-2}$) (100) silicon on insulator (SOI) wafers with top Si thickness (T_{Si}) of 70 nm were used as starting materials. After thinning the T_{Si} to 20 nm, a 40-nm-thick $\text{Si}_{0.75}\text{Ge}_{0.25}$ layer was epitaxially deposited on the thin SOI substrate by UHV chemical vapor deposition at 580 °C. Cyclic oxidation and annealing processes at 750 and 950 °C were used as the first Ge condensation step to one-dimensionally condense Ge into the underlying SOI, forming a uniform SiGe-OI substrate.¹¹ After stripping the thermal oxide, lines down to 120 nm in width were patterned using a 248 nm exposing wavelength KrF scanner. The line-width was further trimmed down to 40–50 nm by a controlled O_2 plasma process. The resist patterns were then transferred into the SiGe layer using a reactive ion etching process to form SiGe fin structures. Subsequently, the wafers were condensed at 875 °C for the second Ge condensation process. Due to geometrical differences, the second condensation proceeded two dimensionally for the SiGe fin regions and one dimensionally for the large S/D pad regions, as illustrated in Fig. 1(a).^{12,13} Therefore, the second condensation step resulted in higher Ge concentration in the SiGe fin regions as compared to the S/D pad regions. The second condensation step essentially converted the SiGe fins into Ge-rich SiGe NWs. From transmission electron microscopy (TEM) energy dispersive spectrometry analysis, it was determined that a horizontal source-channel-drain (S-C-D) heterostructure comprising $\text{Si}_{0.7}\text{Ge}_{0.3}$, $\text{Si}_{0.3}\text{Ge}_{0.7}$, and $\text{Si}_{0.7}\text{Ge}_{0.3}$ was formed, which was subsequently used to form the active regions of the NW FETs. Larger width ($\sim 1 \mu\text{m}$) FETs fabricated on the same wafers serve as the control devices. Due to the uniform width, for reference transistors, homostructure comprising $\text{Si}_{0.7}\text{Ge}_{0.3}$ S-C-D was formed instead. After oxide stripping, the SiGe surface was passivated with an epitaxially grown Si layer less than 2 nm thick. A gate stack comprising $\sim 8 \text{ nm HfO}_2$ and 75 nm TaN was deposited by low power physical vapor deposition. After gate definition, the device

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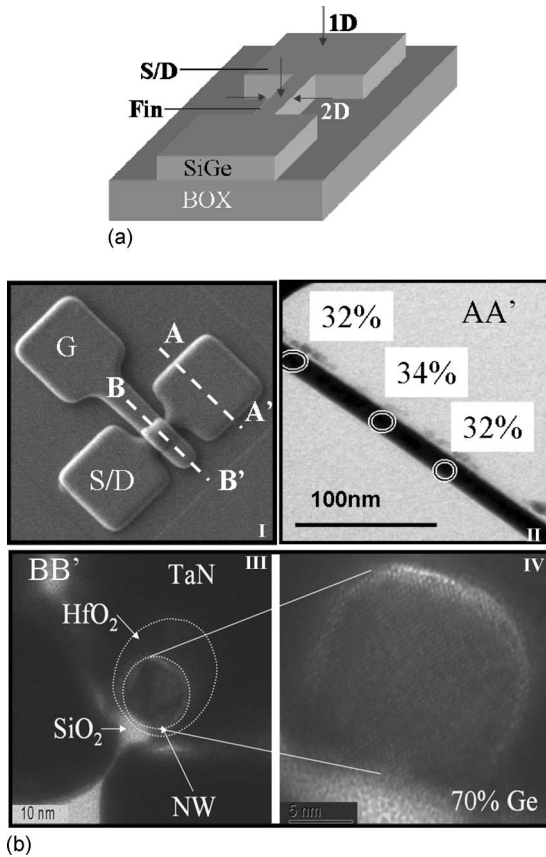


FIG. 1. (a) Schematic view illustrating the pattern-size-dependent Ge condensation technique. (b)(I) shows the SEM image of a completed SGNW FET, with AA' and BB' representing two TEM cutting planes. (b)(II) shows the TEM image of the S/D region for the AA' cut. (b)(III) is the TEM micrograph of the cross section (BB' cut) for the SiGe NW channel. Energy dispersive x-ray spectrometry showing Ge% in SiGe NW is 70%, and the HRTEM image of SiGe NW is shown on the right.

fabrication was completed by BF_2 S/D implant, activation (875 °C), and metallization processes.

Figure 1(b)(I) shows the scanning electron microscopy (SEM) image of a SGNW FET, with gate and S/D regions indicated. AA' and BB' denoted TEM cutting planes for S/D regions and channel regions, respectively. As shown in Fig. 1(b)(II), the Ge concentration is $\sim 30\%$ in the S/D regions (AA' cut) due to one-dimensional Ge condensation. Figure 1(b)(III) shows the cross-section TEM micrograph (BB' cut) of the SGNW channel regions. The SGNW, with a diameter of 13 nm, is covered by 8-nm-thick HfO_2 and 75-nm-thick TaN with some shadowing effect, thus forming an Ω -shaped gate structure. The corresponding high resolution TEM (HRTEM) image of the SGNW is shown in Fig. 1(b)(IV). The SGNW is nearly circular with a Ge concentration of up to 70%. The good crystalline structure of the NW indicates the effective suppression of defect formation by utilizing the Ge condensation method with cyclic annealing.

Figure 2 illustrates the band diagram along the channel direction, with the corresponding schematic view of the device structure on top, for both heterojunction and homojunction devices. As shown in Fig. 2(a), the band gap decreases significantly with higher Ge concentration, as given by $E_g(\text{alloy}) = xE_{g1} + (1-x)E_{g2}$.¹⁴ Without considering any strain effects inside the NW, the band gaps of $\text{Si}_{0.7}\text{Ge}_{0.3}$ and 70% $\text{Si}_{0.3}\text{Ge}_{0.7}$ were calculated to be ~ 0.99 and ~ 0.81 V, respectively. In our process, a nonabrupt heterojunction with

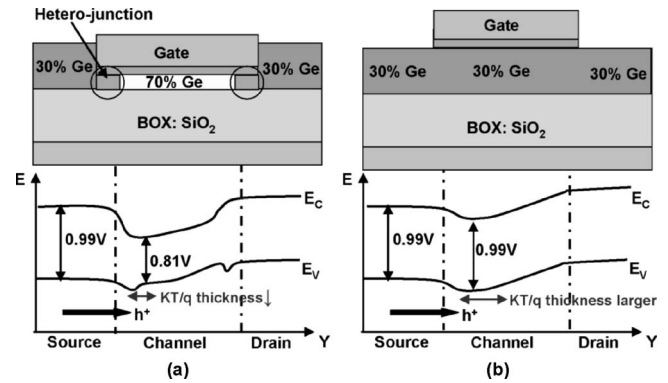


FIG. 2. (a) Schematic view of SiGe NW devices with heterostructures along the channel direction. Ge concentration is modulating in S-C-D, where 30% Ge is in S/D while 70% is in the channel area. The band diagram along the channel direction is shown below. As Ge% varies, the band gap changes from 0.99 V (S/D) to 0.81 V (channel). This results in valence band offset between source and channel, which reduces the KT/q layer thickness from the source toward the channel. (b) shows the schematic of the homostructure for comparison; the KT/q layer thickness is larger compared to heterostructure devices.

graded Ge concentration (indicated in the circle) is formed as a result of the curved S/D extensions and the channel regions due to the corner round effect in fin lithography. Although the heterostructure is nonabrupt, the hole injection velocity from the source into the channel is expected to increase with the excess kinetic energy from the valence band offset. Furthermore, the decreased thickness of the KT/q barrier layer from the channel to the source at a given gate overdrive voltage reduces the probability and proportion of carrier backscattering. For comparison, the schematic of the control planar device is also shown in Fig. 2(b). Due to the uniform Ge concentration along the channel direction, the homostructure has a constant band gap (0.99 V) from the source to the channel region. Thus, a relatively larger KT/q thickness is observed.

To investigate the hole injection enhancement due to the S-C-D heterostructure, the channel backscattering coefficients for both SGNW and planar devices were extracted using a temperature-dependent model.¹⁵ Figure 3 shows the temperature dependence of $I_{D\text{sat}}$ for both SGNW and planar devices with gate length of 350 nm. α is the temperature coefficient of $I_{D\text{sat}}$ obtained from the gradient. α of SGNW is $\sim 32\%$ smaller than that of the control planar device. Next,

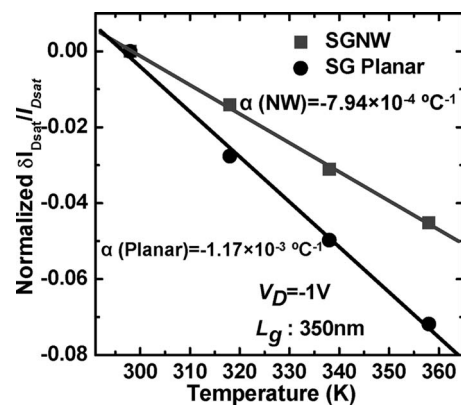


FIG. 3. Drive current change as a function of temperature between SGNW and planar devices at $V_D = -1$ V. The temperature coefficient α of SGNW is 32% smaller than planar devices.

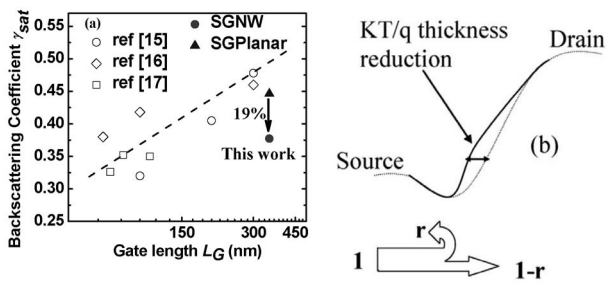


FIG. 4. (a) Comparison of backscattering coefficient for this work and other works (Refs. 15–17). The backscattering coefficient of SGNW was found far below the fitting line at the same gate length. Besides, 19% reduction has been achieved for SGNW devices over planar devices. (b) The band diagram illustrates KT/q layer thickness reducing in 70% Ge channel of SGNW devices.

backscattering coefficient was extracted.^{16,17} Figure 4(a) plots the backscattering coefficient for both SGNW devices and homojunction planar devices. The backscattering coefficients from other works are also shown for comparison. By linearly fitting the reference data and extrapolation toward longer gate length, it becomes obvious that the backscattering coefficient of the SGNW is far below the trend line for the same gate length. Furthermore, the backscattering coefficient γ_{sat} of the SGNW is 19% lower than that of the control planar devices. This confirms that the heterostructure SGNW indeed has enhanced hole injection due to the hole barrier KT/q layer thickness reduction, as shown in Fig. 4(b). The solid line corresponds to the heterostructure, while the dashed line refers to the normal homostructure; for the same KT/q energy reduction, the heterostructure exhibits barrier thickness lowering compared to the homostructures. Channel mobility can also be an important aspect for structure evaluation. However, in view of the reducing number of carriers (charge) in the channel or the reducing gate capacitance due to the small surface area of the NW channel ($C_{area} \sim 3.14 \times 350 \times 13 \text{ nm}^2$), it is difficult to measure the gate capacitance using split C - V to extract the mobility of the SiGe NW. Use of the calculated capacitance value could have been another way, but due to the involvement of high- k dielectric (precise k value unknown) and the rather complex Ω -shaped channel, the capacitance calculations might be far off from the experimental value and might thus lead to inaccuracies in mobility. To abstain from reporting inaccurate mobility numbers, we compared the linear transconductance to investigate the mobility difference between SGNW and planar devices as linear (low lateral field) transconductance, which is directly proportional to mobility. It is found that the peak of linear G_m of SGNW is 4.5 times that of planar devices.⁷ This enhancement is mainly attributed to two factors: First, with higher Ge concentration in the SGNW channel (70%) over planar channel (30%), hole mobility could be enhanced due to the larger intrinsic hole mobility property of Ge. Besides, with the energy band modulation of SGNW, a valence band offset ΔE_V is formed from the source to the

channel region, which could further increase hole velocity due to the excess kinetic energy. Apart from these, there could also be some other factors accounting for the hole mobility enhancement of SGNW devices: Ω -shaped structure for better gate controllability and strain effect along the NW channel direction. Although it would be difficult to extract the mobility of the NW channel due to limitations in the measurement facilities and device layout designs, the mobility investigation of the NW channel would be an interesting topic for future nanoscale device explorations.

In summary, SGNW transistors were fabricated using a two-step pattern-size-dependent Ge condensation technique, which resulted in the formation of the S-C-D heterostructure. This reduced the hole KT/q barrier layer thickness from source to channel, which enhances the carrier injection from source to channel. This was confirmed by performing temperature-dependent carrier backscattering characterization.

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