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## Fabrication of thick SiGe on insulator ( $\text{Si}_{0.2}\text{Ge}_{0.8}\text{OI}$ ) by condensation of SiGe/Si superlattice grown on silicon on insulator

S. Balakumar,<sup>a)</sup> S. Peng, K. M. Hoe, G. Q. Lo, R. Kumar, N. Balasubramanian, and D. L. Kwong  
*Institute of Microelectronics, 11 Science Park Road, Singapore Science Park II, Singapore 117685, Singapore*

Y. L. Foo and S. Tripathy  
*Institute of Materials Research and Engineering, 3 Research Link, Singapore 117602, Singapore*

(Received 7 February 2007; accepted 12 April 2007; published online 9 May 2007)

In this work, the authors demonstrate a fabrication methodology for obtaining a thick ( $\sim 250$  nm) high Ge content SiGe-on-insulator (SGOI) film. About 800 nm thick low Ge content ( $\sim 25\%$ ) SGOI film was fabricated by intermixing SiGe and Si through thermal annealing of a superlattice comprising of 60 periods of  $\text{Si}_{0.7}\text{Ge}_{0.3}$  and Si on silicon-on-insulator (SOI) substrate. A combination of oxidation and annealing processes was used to condense and diffuse the Ge through SiGe film to obtain thick  $\text{Si}_{0.2}\text{Ge}_{0.8}\text{OI}$ . It is also found that the oxidation termination is due to residual stress in the thick SGOI layer. The transmission electron microscopy measurements showed that the  $\text{Si}_{0.2}\text{Ge}_{0.8}\text{OI}$  film exhibits a single crystalline nature with an orientation that is the same as the starting SOI. X-ray diffraction measurements confirmed that the in-plane strain of the SGOI layers is compressive or nearly relaxed. © 2007 American Institute of Physics. [DOI: 10.1063/1.2737818]

Si/Ge heterostructures on SiGe-on-insulator (SGOI) substrates are promising templates for high-speed electronic devices, Si-based optoelectronic integrated circuits<sup>1</sup> (OEICs) and Ge metal-oxide-semiconductor field-effect transistors.<sup>2</sup> High Ge content SiGe is also a suitable material for infrared photodetectors due to its compatibility with Si technology; it has a narrow band gap with a much larger absorption coefficient in the infrared region than that of Si. Thus, OEIC optical devices can be monolithically integrated with the SiGe high-speed electronic devices on SGOI substrates. Tezuka *et al.*<sup>3</sup> reported the SGOI fabrication technique based on Ge condensation through the selective oxidation of Si of deposited SiGe on silicon on insulator (SOI). It has become a popular technique to fabricate substrates for complementary metal-oxide semiconductor (CMOS) technology as the composition, the strain, and thickness can be effectively controlled as compared to other techniques.<sup>3</sup> Koh *et al.* used a thin condensed SGOI as a template for the growth of thick SGOI to fabricate OEIC devices.<sup>1</sup> In this juncture, we made an effort to fabricate thick SGOI by condensation itself so that graded layer could be avoided. It is also desirable to investigate the material structures and the strain characteristics of thick single crystalline SGOI layer prepared by Ge condensation. This could result in high Ge content templates for optoelectronic device application. However, there are challenges related to the formation of high Ge content SGOI or germanium-on-insulator films.<sup>4-7</sup>

It is possible to achieve a uniform thin layer of high Ge content SGOI with appropriate oxidation/annealing steps.<sup>5</sup> For optical application, 0.1 to 0.4  $\mu\text{m}$  of high Ge content SGOI-based layers are needed, depending on the incident light direction and wavelength. The fabrication of high Ge concentration thick SGOI films can only be achieved by first fabricating a thick layer of SiGe with nominal Ge ( $\sim 25\%$ )

followed by condensation to get a high Ge content SGOI film. To get such a thick film, in this work, we introduced a method of intermixing the  $\text{Si}_{0.7}\text{Ge}_{0.3}$ /Si superlattices (SLs) by means of the annealing process. Then, it was used to fabricate high Ge content SGOI film. The strain characteristics in these SGOI films are investigated using x-ray diffraction technique.

Figure 1 shows the schematic representation of SL structure, thick SGOI layer, and the final layer after condensation. Since the target is to achieve thick SiGe film with  $>80\%$  of Ge content, a very thick starting layer (800 nm) with about 25% Ge concentration is preferred prior to condensation. To obtain a high quality thick crystalline layer, 60 periods of  $\text{Si}_{0.70}\text{Ge}_{0.30}$ /Si SLs are first grown on thin SOI wafer using an ultrahigh vacuum chemical vapor deposition system (Fig. 2). The SOI overlayer thickness was around 35 nm and the buried oxide thickness was 1450 Å. The high resolution transmission electron microscopy (HRTEM) images of SLs [Fig. 2(a)] show the thicknesses of SiGe and Si within the period to be about 12 and 3 nm, respectively. The preoxidation of SLs for 15 min was carried out to avoid Ge loss during subsequent annealing. About 5 h of annealing the SLs resulted in an  $\sim 800$  nm thick SGOI film with  $\sim 25\%$  Ge concentration, as shown in Fig. 2(c). About 10 000 SCCM (SCCM denotes cubic centimeter per minute at STP) of oxy-

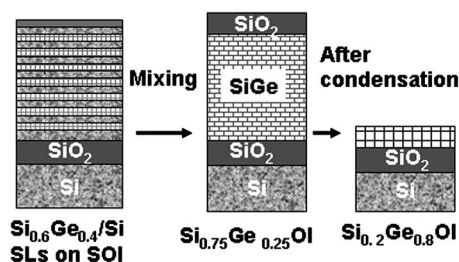


FIG. 1. Schematic representation of (a) SiGe/Si SLs deposited on SOI, (b) the thick layer of SGOI, and (c) condensed  $\text{Si}_{0.8}\text{Ge}_{0.2}\text{OI}$ .

<sup>a)</sup>Electronic mail: subra@ime.a-star.edu.sg

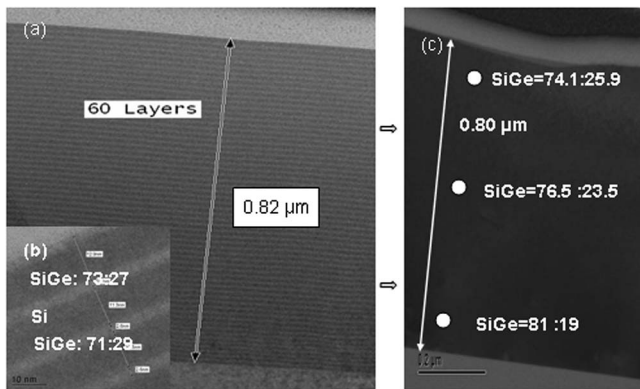


FIG. 2. Cross-sectional TEM images of (a) SiGe/Si SLs, (b) HRTEM image of SiGe/Si SL, and (c) TEM image after 30 min of oxidation and annealing.

gen is used during oxidation and 15 000 SCCM of nitrogen is used for annealing. TEM analysis confirmed that the bottom part of the layer has less Ge (19%) due to the intermixing of the thicker 35 nm SOI with subsequently deposited SiGe/Si layers [Fig. 2(c)].

Consequently, oxidation was carried out at 1050 °C for a total duration of 10 h with intermittent annealing of 1 h for each hour of oxidation step. Also, in this process, the oxide formed was etched after every 3 h of oxidation as self-limiting oxidation was observed once the oxide thickness exceeds  $\sim 1300$  Å.<sup>8</sup> Figure 3(a) shows the cross-sectional TEM image of thick SGOI layer with 37% of Ge content after the initial 10 h of oxidation. Further, 20 h of oxidation at 1050 °C increased the Ge content to 57% with about 5% gradient across thickness of the film [Fig. 3(b)]. The process time is longer due to self-limited oxidation at lower concentration of Ge. Once the Ge concentration reaches  $\sim 60\%$ , oxidation temperature was reduced to 1000 °C for better control of the oxidation process. The oxidation and annealing were further carried out for additional hours. This increased the Ge concentration to  $\sim 70\%$  in the first 2 h of oxidation/annealing and beyond this concentration; the intermittent annealing was introduced every half an hour to avoid the interface melting and SiGeO formation.<sup>5</sup>

Further oxidation was carried out at 950 °C (2 h) and 900 °C (1 h) with multiple oxidation steps along with 15 min intermittent annealing to achieve SGOI with Ge content around 80%. Figure 3(c) shows that the thickness of Si<sub>0.2</sub>Ge<sub>0.8</sub>OI is about 250 nm. This is the thickest layer with such a high Ge content SGOI reported so far. HRTEM analysis shows a high quality crystalline SGOI with low defect density. After mixing the SLs, if there is insufficient preannealing, the defect counts were found to be very high, mostly horizontal line defects and dislocation densities were observed. These huge numbers of defects appeared due to strain relaxation in the Ge graded layers. In SGOI, mostly 60° dislocation lines will appear if preannealing is insufficient. In this work, we studied the effect of condensation on dislocation density with and without preannealing. A preannealing of 5 h at 1050 °C resulted in a reduction of the dislocation density and their propagation. The defect formation depends on layer thickness, Ge concentration, and annealing temperature.

Two different mechanisms are proposed to address self-limiting oxidation of SGOI.<sup>3,7</sup> Tezuka *et al.*<sup>3</sup> proposed that it might be due to residual stress generated by Ge gradient in

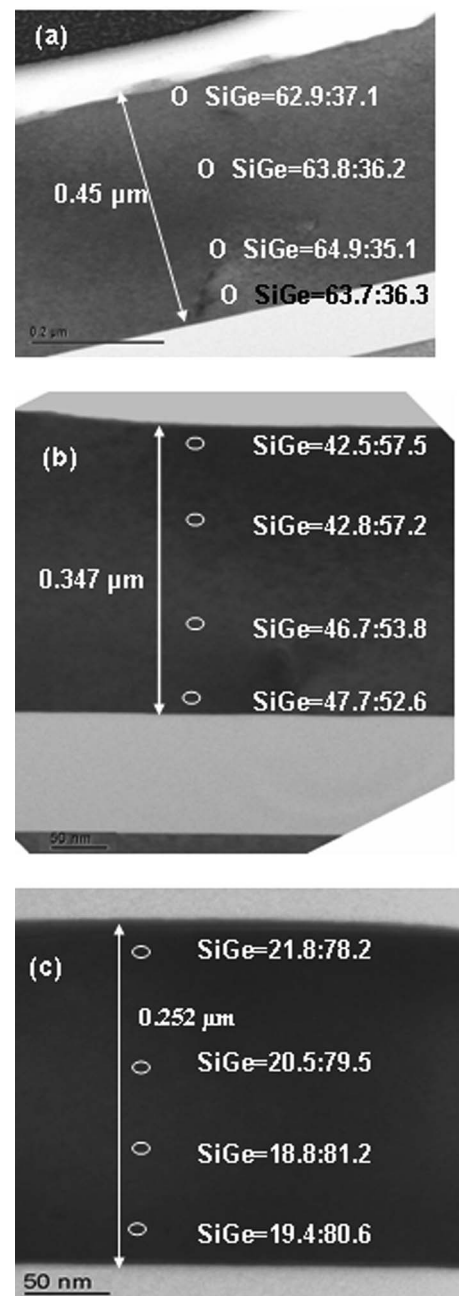


FIG. 3. Sequential TEM images of condensation process for SGOI with (a) 37% of Ge, (b) 57% of Ge, and (c) 80% of Ge.

the SiGe layer and commented that more studies are required to identify the mechanism. A recent report<sup>7</sup> predicted that self-limiting oxidation is due to the melting of an interfacial layer that has a high Ge concentration between the surface oxide and the SiGe layer. In the present study, oxidation was carried out with 1 h intermittent annealing for every 1 h oxidation to diffuse the Ge towards the bottom of SiGe. However, we observed that oxidation termination occurred once the oxide thickness exceeded 1300 Å though sufficient intermittent annealing was applied. It is confirmed that the oxidation limiting issue is not due to the high Ge content interfacial layer. On the contrary, Ge diffusion at this temperature across the layer is still not enough to relieve the residual thermal stress gradient across the thick SiGe ( $\sim 500$  nm). It also does not allow the Si to appear in the interface to oxidize. In our earlier studies, a thin S<sub>0.1</sub>G<sub>0.9</sub>OI layer was fabricated with 150 nm SiGe on SOI without intermittent oxide

TABLE I. Lattice constants and strain values from x-ray data.

Ge composition	As annealed	~37%	~46%	~80%
In-plane lattice constant	5.495	5.500	5.521	5.527
Out of plane lattice constant ( $a_L$ )	5.511	5.501	5.528	5.628
Relaxed lattice constant ( $a_L$ )	5.504	5.501	5.525	5.628
In-plane strain (%)	-0.163	-0.01	-0.071	-0.01

etching.<sup>5</sup> In that case, oxidation occurred even when the oxide thickness increased to 3000 Å on SiGe but the number of oxygen radicals arriving to the interface was lowered with the increase of oxide thickness. Hence, the mechanism depends on the SiGe layer thickness, Ge content thermal stress gradient in the layer, and oxide layer thickness. Further studies are needed for different SiGe layer thicknesses and different Ge contents at low and high temperatures.

Next, the strain in the fabricated thick SGOI layers was evaluated using high-resolution x-ray diffraction (XRD) technique. The high resolution rocking curve and reciprocal lattice map measurements were performed with line-focused Cu  $K\alpha_1$  radiation ( $\lambda=1.5406$  Å). The lattice parameters are extracted from (004) and (224) reciprocal lattice map as well as and rocking curve analyses. The extracted lattice parameters along the parallel ( $a_l$ ) and perpendicular ( $c_l$ ) directions were used to calculate the relaxed lattice parameter of SGOI layers using<sup>8</sup> the relationship  $a_L=c_l[1-2\nu(c_l-a_l)/(1+\nu)c_l]$ , where  $\nu$  is the Poisson ratio. The in-plane strain was determined using the relation  $\epsilon_{xx}=(a_l-a_L)/a_L$ . All the lattice constants and in-plane strain values of SGOI are shown in Table I. It is found that the in-plane strain components in all the layers are compressive whereas the as-annealed superlattices are more compressive than the condensed layers since 5 h nitrogen annealing is not sufficient enough to release the strain. The fluctuation in the strain values is due to the use of number of Ge condensation/annealing thermal cycles, and

prolonged annealing relaxed the layers. It is confirmed that relaxed or compressive layer can be easily fabricated through the condensation technique with sufficient thermal cycles. Thus, such a method can be used to fabricate high Ge content SGOI templates. It is also possible to thin down the layer by chemical mechanical polishing to the required thickness for use in CMOS platforms.

In summary, about 250 nm thick highly strain relaxed  $\text{Si}_{0.2}\text{Ge}_{0.8}\text{OI}$  layer is fabricated by a condensation technique through intermixed SiGe/Si SLs deposited on SOI. The intermixing of SiGe/Si SLs by annealing could be the best way to get a starting thick SiGe layer on insulator. Utilizing such a thick layer, it is possible to fabricate thick SGOI layers with more than 80% Ge. Oxidation saturation/termination is observed due to residual stress in the SiGe layer. The XRD and micro-Raman scattering studies show the presence of a much lower in-plane residual compressive strain in such layers. Such SGOI templates may find applications in photodetectors and MOS devices.

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