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## Time dependent thermoelectric performance of a bundle of silicon nanowires for on-chip cooler applications

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With finite element simulation, the time dependent thermoelectric performance of silicon nanowires (SiNWs) is studied systematically. Short response time has been observed in SiNW cooler which decreases with increasing of the number of SiNWs. Moreover, the impacts of inhomogeneous thermal conductivity distribution in one bundle on the cooling temperature have been studied. The cooling temperature decreases due to the existing of unexpected high thermal conductivity SiNW. This impact can be suppressed in large system. Our results provide a comprehensive performance analysis of SiNWs for on-chip thermoelectric cooler applications. © 2009 American Institute of Physics. [doi:10.1063/1.3273869]

Microelectronic devices can generate huge heat fluxes in very small areas (also called hot-spot). Typical integrated circuit (IC) chips have dozens of millions of transistors. The hot spots in ICs are normally in the order of 300–400  $\mu\text{m}$  in diameter, thus even the smallest commercial cooling module is still too large for spot cooling. As the silicon stacked chips or three-dimensional chips are in rapid development, this would create smaller and hotter spots. The current cooling technologies are fast reaching their limits. So an efficient nanoscale cooler would play a crucial role in the thermal management of future ICs. Among nanoscale thermoelectric (TE) materials, silicon nanowires (SiNWs) are of crucial importance.<sup>1,2</sup> A good thermoelectric material must have a high figure of merit ( $ZT$ ), which is proportional to the Seebeck coefficient ( $S$ ), electrical conductivity, and absolute temperature, but inversely proportional to thermal conductivity. In SiNWs, the electrical conductivity and electron contribution to Seebeck coefficient are similar to those of bulk silicon,<sup>3–5</sup> but exhibit 100-fold reduction in thermal conductivity,<sup>6–9</sup> showing an approximately 100-fold improvement of the  $ZT$  values over bulk Si in a broad temperature range.<sup>1,2</sup> This has raised the exciting prospect that SiNWs can be applied as nanoscale thermoelectric materials. SiNWs are appealing choice also because of their small sizes and ideal interface compatibility with conventional Si-based technology. In a previous study,<sup>10</sup> by using finite element simulation and analytic modeling, we have investigated the steady-state performance of individual SiNWs. Large cooling temperature, high cooling power density, and high cooling coefficient are observed. Moreover, the cooling temperature increases remarkably as thermal conductivity of SiNW decreases. However, for practical applications, a bundle of SiNWs is more commonly used as they generate larger cooling power. Furthermore, the cooling response time is another important factor for a TE cooler which was not investigated with the steady-state analysis in our earlier work. By including the above mentioned factors, here we present a more comprehensive investigation on the time dependent cooling performance of SiNWs, including the cooling response time, the impact of number of SiNWs in the bundle, and the influ-

ence of inhomogeneous thermal conductivity distribution in the bundle.

It is well known that one-dimensional structures have obviously different thermal properties from bulk material. For instance, in a carbon nanotube, heat conduction does not obey the Fourier law, and the thermal conductivity depends on the length.<sup>11–13</sup> However, it has also been demonstrated that when the SiNW length is in micrometer range, then classical transport models can be used with experimental parameters to describe the thermal properties of nanostructured silicon system accurately. These results are in good agreement with experimental observations.<sup>14</sup>

In this letter, we perform the numerical simulation based upon macroscale heat transfer models (e.g., Fourier law for heat conduction) with experimental reported material properties. Our simulations are based on a model that SiNWs are in contact with a silicon island (both are suspended), this island corresponds to a microprocessor or a hot spot. The size of SiNW is 50 nm  $\times$  50 nm  $\times$  2.5  $\mu\text{m}$ , and the size of the silicon island is 20  $\mu\text{m}$   $\times$  20  $\mu\text{m}$   $\times$  200 nm. The number of SiNWs is  $N$ . These dimensions are in the range of the experimental observation. The cross section of SiNW is square geometry which is easy to be fabricated by top-down techniques on silicon-on-insulator (SOI) substrates. On passing electrical current, electrons absorb thermal energy from the lattice at one junction and transport it to another junction, creating a cold and hot side. Here the silicon island is assumed to be in contact with the cold side and the other side (hot side) is fixed at 300 K. This is well known as Peltier effect, which can decrease the temperature of the silicon island. Besides this positive cooling effect, the back-flow of heat from hot end to cold end and Joule heat will weaken the cooling efficiency. In our model, heat flux is the sum of Seebeck (Peltier) effect, Fourier effects, and the Joule heat. Figure 1 shows the schematics of the cooling calculation model. The governing equation which represents the heat transfer in the SiNW is as follows:

$$\nabla \cdot (-\kappa \cdot \nabla T + S \cdot T \cdot J) = J \cdot (-\nabla \cdot V) - c \frac{\partial T}{\partial t}, \quad (1)$$

where  $k$ ,  $S$ , and  $T$  are the thermal conductivity, the Seebeck coefficient, and the temperature, respectively.  $J$  and  $V$  are the

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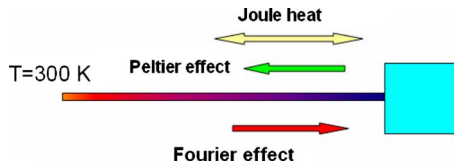


FIG. 1. (Color online) The schematics of the cooling calculation model.

applied electrical current density and the electrostatic potential, respectively.  $c$  is the thermal capacity. In our simulations, the experimental reported material properties of SiNW are used. The Seebeck coefficient, thermal conductivity and electrical resistivity of SiNW are chosen as  $245 \mu\text{V}/\text{K}$ ,  $1.6 \text{ W}/\text{m K}$  and  $1.7 \times 10^{-5} \Omega \text{ m}$  at  $300 \text{ K}$ , respectively.<sup>1</sup> Natural convection and radiation as the heat transfer mechanism between the system and the surrounding air are established. The surrounding environment is assumed to be stationary air at atmospheric pressure. Electrical bias is applied across the single SiNW to generate current. COMSOL MULTIPHYSICS,<sup>15</sup> a finite element analysis program with the electrical and thermal modules, is used to perform this time-dependent thermal analysis of the system to evaluate the cooling temperature and response time of performance.

Figure 2(a) shows the time dependent temperature of the Si island. Upon current flow through the SiNW, the temperature of the island decreases exponentially initially and then converges to a constant temperature  $T_C$  which is much lower than the environment temperature  $T_0$ . The cooling temperature  $\Delta T = T_0 - T_C$ . It is worth pointing that the temperature decrease depends on the operating current remarkably. As the current increases the cooling temperature  $\Delta T$  increases and reaches a maximum at about  $I_M = 3.0 - 4.0 \mu\text{A}$ . Above  $I_M$ , cooling temperature decreases with increasing current. An increase in electrical current will absorb more thermal energy from one end and transport it to another end; on the other hand, the increase of electrical current will also increase Joule heating that in turn will increase the heat flux to the cool end, thus suppress cooling. For a SiNW, in the low electrical current regime, the Joule heating is small, thus the

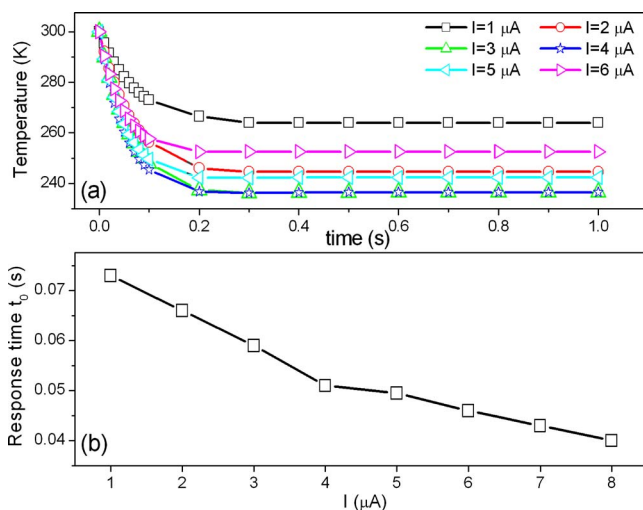


FIG. 2. (Color online) (a) Time dependent temperature of the Si island for different applied electrical current. The temperature decreases with time exponentially:  $T(t) = T_C + \Delta T e^{-t/\tau}$ , here  $T_C$  is the stationary-state temperature of the island,  $\Delta T = T_0 - T_C$  is the cooling temperature,  $T_0$  is the environment temperature,  $\tau$  is the response time. (b) Dependences of cooling response time on applied electrical current.

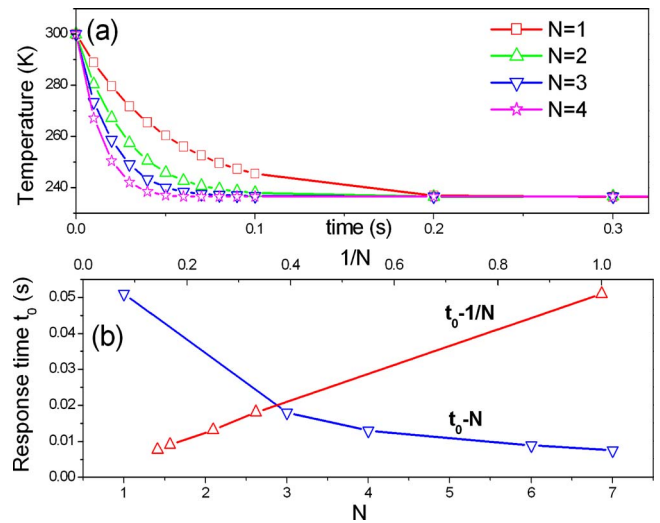


FIG. 3. (Color online) (a) The time dependent temperature for different number of SiNWs  $N$ . (b) The cooling response time  $t_0$  for different number of SiNWs  $N$ . Here the electrical current is  $4 \mu\text{A}$ .

cooling temperature increases with increasing electrical current. However, in the high electrical current regime, as more and more Joule heat is generated which is proportional to the square of the current, it results in the decrease of cooling temperature as electrical current is increased.

From the best fitting of the time dependent temperature curves, the cooling response time  $t_0$  can be calculated. Figure 2(b) shows that  $t_0$  decreases as applied electrical current increases monotonously. From Fig. 2(a), the maximum cooling temperature can be achieved with about  $3 - 4 \mu\text{A}$  electrical current, with response time of  $0.05 - 0.06 \text{ s}$ , which corresponds to about  $1 \text{ ms}/\text{K}$ . It is much shorter than those observed in commonly used BiTe ( $10 \text{ ms}/\text{K}$ ) and  $(\text{Bi}, \text{Sb})_2(\text{Te}, \text{Se})_3$  ( $4 \text{ ms}/\text{K}$ ) TE devices.<sup>16,17</sup> This demonstrates that SiNW is a fast response cooler.

The results shown above are the cooling performance of individual SiNW; in practical application, a bundle of SiNWs will be used, which can be realized by top-down method on SOI wafers. Figure 3 shows the time dependent temperature of the silicon island with a number of SiNWs  $N (> 1)$ . With increase in  $N$ , the cooling process becomes faster. However, the maximum  $\Delta T$  does not change with  $N$ . Figure 3(b) shows the  $N$  dependent response time. It is obvious that in practical applications, increasing of  $N$  is an efficient approach to speed the cooling process.

It has been demonstrated that large thermal conductivity reduces TE cooling temperature.<sup>10</sup> The thermal conductivity of SiNW depends on the surface roughness and transverse dimension. Different thermal conductivity values are reported experimentally. For instance, for SiNW with  $50 \text{ nm}$  diameter, from  $1.6$  to about  $20 \text{ W}/\text{m K}$  are observed which depends on the surface roughness.<sup>1,7</sup> In practical SiNWs, such as the wafer-scale arrays of SiNWs synthesized by aqueous electroless etching method, the surfaces roughness of SiNWs can be very different, and induces inhomogeneous thermal conductivity distribution in one bundle. So it is indispensable to investigate the impact of randomly high thermal conductivity on the cooling performance of the entire cooling setup. Now in the  $N$ -SiNW bundle, there exists two values of thermal conductivity:  $\kappa_0$  and  $\kappa_1$ .  $\kappa_1$  is the unexpected high thermal conductivity of one NW which changes

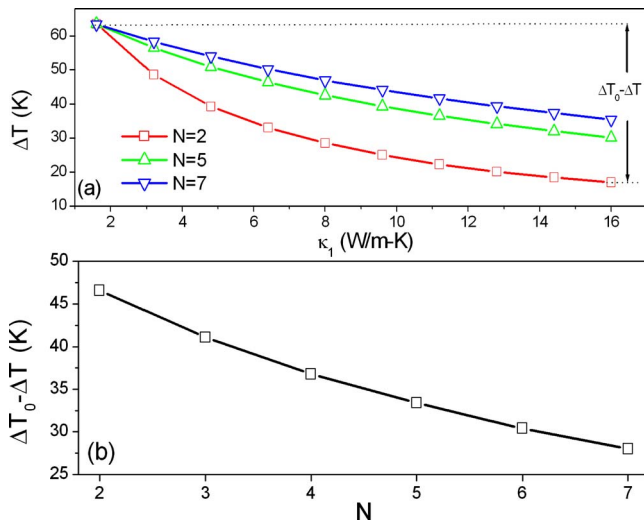


FIG. 4. (Color online) (a) Impact of unexpected high thermal conductivity of one SiNW in the  $N$ -wire bundle on the cooling performance.  $\kappa_1$  is the unexpected high value of thermal conductivity. (b) Influence of one high thermal conductivity SiNW on the cooling temperature of the whole  $N$ -wire bundle. This influence decreases with increasing of the number of SiNWs exponentially.

from 1.6 to 16 W/m K, while  $\kappa_0$  is the thermal conductivity of all other SiNWs with  $\kappa_0=1.6$  W/m K. As shown in Fig. 4(a), with  $\kappa_1$  increases, the cooling temperature  $\Delta T$  decreases remarkably, demonstrating the negative impact of high thermal conductivity on cooling performance. With increasing of  $N$ , the negative impact of  $\kappa_1$  decreases quickly as the role of one high thermal conductivity NW is relatively suppressed in large system. Figure 4(b) shows the influence of inhomogeneous thermal conductivity distribution on the cooling temperature of the whole SiNW bundle. Here  $\Delta T_0$  is the cooling temperature when thermal conductivity of all wires in the bundle is  $\kappa_0=1.6$  W/m K, and  $\Delta T$  is the cooling temperature when thermal conductivity of one SiNW is 16 W/m K.  $\Delta T_0 - \Delta T$  represents to the negative impact of one unexpected high thermal conductivity SiNW on the cooling temperature. It decreases with  $N$  exponentially. The best fitting

relation is:  $\Delta T_0 - \Delta T = 17.8 + 43.5e^{-N/N_0}$ , where  $N_0=5$ . For  $N \gg 5$ , the cooling temperature of the inhomogeneous bundle is about 17.8 K lower than that of a bundle with uniform thermal conductivity of 1.6 W/m K. Our results demonstrate that in practical applications, a bundle of SiNWs with  $N \gg 5$  is required to suppress the influence of inhomogeneous thermal conductivity distribution.

A systematic time dependent investigation on the thermoelectric performance of SiNWs has been performed. Short response time has been achieved in SiNW cooler which can be reduced further by increasing the number of SiNWs in the bundle. Moreover, we investigated the impacts of inhomogeneous thermal conductivity distribution in one bundle on the cooling temperature. The cooling temperature decreases due to the existing of unexpected high thermal conductivity SiNW in the bundle. This impact can be suppressed in large system. Our results demonstrate that in thermoelectric cooling applications, a bundle of SiNWs with a large number of wires is preferred.

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