Strained n-Channel FinFETs Featuring *In Situ* Doped Silicon–Carbon ($\mathrm{Si}_{1-y}\mathrm{C}_y$) Source and Drain Stressors With High Carbon Content

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***Abstract*—Phosphorus *in situ* doped $\mathrm{Si}_{1-y}\mathrm{C}_y$ films (SiC:P) with substitutional carbon concentration of 1.7% and 2.1% were selectively grown in the source and drain regions of double-gate ⟨110⟩-oriented (110)-sidewall FinFETs to induce tensile strain in the silicon channel. *In situ* doping removes the need for a high-temperature spike anneal for source/drain (S/D) dopant activation and thus preserves the carbon substitutionality in the SiC:P films as grown. A strain-induced I_{Dsat} enhancement of ∼15% and ∼22% was obtained for n-channel FinFETs with 1.7% and 2.1% carbon incorporated in the S/D, respectively.**

***Index Terms*—FinFET, *in situ* doped, multiple-gate field-effect transistor (MuGFET), silicon–carbon, strain, stress.**

I. INTRODUCTION

CARBON can be incorporated into substitutional sites in the silicon lattice, not unlike germanium in silicon–germanium alloys. The incorporation of relatively small amounts of substitutional carbon into silicon results in a large lattice mismatch between the silicon–carbon alloy $\mathrm{Si}_{1-y}\mathrm{C}_y$ and silicon. Previously, $\mathrm{Si}_{1-y}\mathrm{C}_y$ films with up to 1% substitutional carbon have been exploited in source/drain (S/D) stressor-induced strained-silicon technology for both planar transistors [1]–[5], as well as multiple-gate transistors, such as FinFETs [5]–[8], resulting in significant I_{Dsat} enhancement. Such enhancement has been attributed to an increase in electron mobility, as a result of the tensile stress induced in the channel [9]. However, it is important to note that the solid solubility of carbon in silicon is extremely low [10]. While it is possible to substitutionally incorporate carbon above the solid solubility limit in silicon–carbon films using nonequilibrium epitaxial growth processes, subsequent high-temperature processes such as S/D dopant activation anneals can cause the loss of carbon substitutionality in these metastable films via the formation of silicon–carbide precipitates [11]–[13]. Naturally, the loss of carbon substitutionality will cause a decrease in tensile channel strain. As such, the thermal instability places a limit on the performance enhancement of devices with implantation-doped $\mathrm{Si}_{1-y}\mathrm{C}_y$ S/D stressors. Besides scaling up the $\mathrm{Si}_{1-y}\mathrm{C}_y$ S/D stressor thickness and increasing the proximity between the stressor and the channel regions [8], or mechanically increasing the lattice strain coupling from the S/D stressors to the channel [14], it is highly desirable to find alternative ways of easily scaling up the channel stress induced in such transistors. *In situ* doped $\mathrm{Si}_{1-y}\mathrm{C}_y$ S/D stressors have the potential of achieving high channel stress, but there are very few reports on the electrical characteristics of transistors with *in situ* doped $\mathrm{Si}_{1-y}\mathrm{C}_y$ S/D stressors.

In this paper, we show that SiC:P films with high substitutional carbon concentration (1.7 at.% and 2.1 at.%) can be employed to induce even larger strain in the channel regions of FinFETs than was previously possible using an implantation-doped epitaxial S/D stressor [6]. The reason is that the S/D stressors being *in situ* doped renders further S/D dopant activation anneals unnecessary. Unlike prior work, where $\mathrm{Si}_{1-y}\mathrm{C}_y$ stressors were implanted and annealed to form the S/D [1], [2], [4], [6]–[8], *in situ* doped $\mathrm{Si}_{1-y}\mathrm{C}_y$ S/D stressors do not need the high-temperature S/D activation anneals that could reduce carbon substitutionality. This allows the preservation of the high substitutional carbon concentration of the stressor film in its as-grown state, in which the carbon percentage is determined by the epitaxial growth process conditions. The incorporation of exceedingly high carbon content for maximum-lattice-mismatch-induced strain is therefore possible. This paper provides an extensive study on the electrical characteristics of FinFETs with $\mathrm{Si}_{1-y}\mathrm{C}_y$ S/D stressors that are

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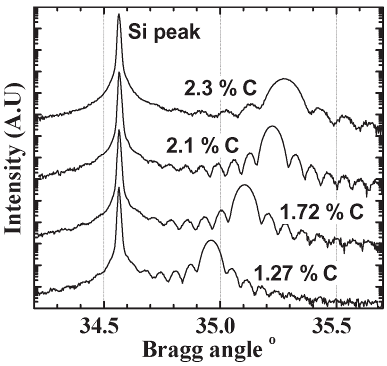

Fig. 1. HRXRD rocking curve of SiC:P films with various substitutional carbon percentages showing excellent crystallinity in the films, despite the high carbon content.

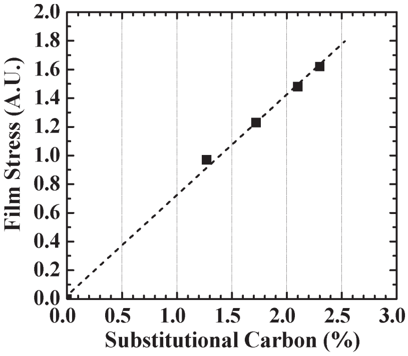

Fig. 2. Wafer curvature measurements indicate a linear relationship between film stress and substitutional carbon percentage in the SiC:P films. This implies that higher stress can be obtained in the FinFET channel regions by incorporating SiC:P S/D stressors of higher substitutional carbon percentages.

- Channel Implant
- Fin definition
- Poly-Si/SiO$_2$ (20Å) gate-stack formation
- Gate definition
- Source/drain extension (SDE) implant
- Spacer formation with stringer removal
- SDE RTA implant activation
- **Spacer liner oxide undercut (wet etching)**
- **Selective Epitaxy Splits:**
  Si:P: P-doped Si (Control)
  SiC:P 1.7%: P-doped $Si_{0.983}C_{0.017}$
  SiC:P 2.1%: P-doped $Si_{0.979}C_{0.021}$

Fig. 3. Process sequence showing key steps employed in FinFET device fabrication. DG FinFETs were fabricated. The gate spacer formation scheme involves an extra *in situ* etch to remove fin spacers, allowing the formation of extended Π-shaped S/D stressors.

in situ doped with phosphorus, i.e., SiC:P, and the performance enhancement that can be achieved with such S/D stressors.

II. *In Situ* Phosphorus-Doped Silicon–Carbon (SiC:P) Films

The phosphorus-doped $Si_{1-y}C_y$ layers (SiC:P) in this paper were grown in an Epsilon reduced-pressure chemical-vapor-deposition epitaxial deposition tool manufactured by ASM. The growth precursors comprised Silcore (ASM trademarked version Si_3H_8), (Mono-) methylsilane (20% MMS in H_2), and PH_3 (1% in H_2), respectively. Silcore, being a precursor with efficient decomposition at low temperatures, is ideally suited for the incorporation of large amounts of substitutional carbon concentration C_{sub} ($> 2\%$). Increasing the substitutional carbon concentration in SiC:P films increases its lattice mismatch with Si, therefore leading to higher SiC:P film stress.

Films with various percentages of substitutional carbon were grown and characterized using high-resolution X-ray diffraction (HRXRD). The HRXRD rocking curves reveal high carbon substitutionality in the SiC:P films of up to 2.3% (Fig. 1). The clearly observable fringe patterns also suggest that these films possess excellent crystallinity. In lattice-mismatched SiGe films grown on Si, it is well established that the critical thickness, beyond which strain relaxation via a dislocation-mediated mechanism would occur, reduces with higher Ge concentration (higher lattice mismatch) [15], [16]. Increasing the C concentration in SiC:P films could also result in a similar behavior due to the increasing lattice mismatch and strain energy. It is expected that such dislocation-mediated strain relaxation would be undesirable for both silicon–germanium and silicon–carbon S/D stressor films in strained transistors, as strain levels in the channel will decrease. To investigate the possibility of dislocation-mediated strain relaxation of high-C-content SiC:P S/D films in typical CMOS strain engineering applications, 50-nm-thick SiC:P blanket films with various carbon percentages were grown on bulk Si wafers. Film stress measurements reveal a linear relationship between SiC:P film stress and substitutional carbon percentage, as shown in Fig. 2. Clearly, this linear relationship indicates that no plastic relaxation has occurred. This implies that the metastable critical thickness has yet to be reached for the SiC:P films at the growth temperatures and seems to be the case even for the SiC:P film with 2.3% substitutional carbon. As long as this linear relationship between stress and carbon percentage is maintained, stress levels in the transistor's channel can easily be tuned or scaled by adjusting the carbon percentage in the SiC:P film.

III. Fabrication of N-FinFETs With SiC:P S/D Stressors

For this experiment, double-gate (DG) (110)-sidewall FinFETs were fabricated on silicon-on-insulator (SOI) wafers using a FinFET process flow that is essentially similar to that described in [6]. Fig. 3 shows the key steps in the process flow. The gate stack comprises 20 Å of thermally grown SiO_2 gate oxide and phosphorus-doped polysilicon gate. After S/D extension (SDE) implant and activation, *in situ* doped SiC:P raised S/D stressors were grown. This simultaneously forms the highly doped S/D regions. Three splits employing different S/D epitaxial films were fabricated in this paper.

In planar MOSFETs employing SiC:P S/D stressors, defects can occur at the corner of the S/D recess due to the growth rate differences for different crystalline orientations. This makes the S/D recess shape critical for obtaining good epitaxial quality in planar MOSFETs [17]. For FinFETs, it has been shown that, even without S/D embedding, Π-shaped Si:C S/D stressors can effectively strain the channel regions for significant performance enhancement [6]. A similar scheme is utilized in this paper. Hence, since the S/D recess etch is omitted in FinFETs,

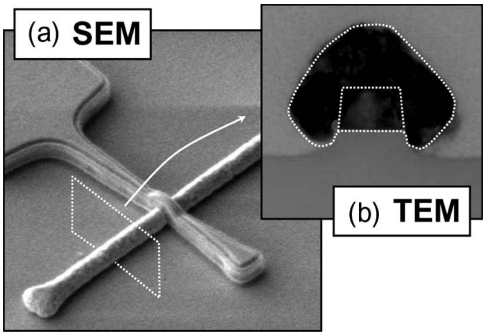

Fig. 4. (a) Isometric-view SEM image showing the selective epitaxial growth of SiC:P with 1.7 at.% of substitutional carbon concentration (also denoted as "SiC:P 1.7%" in subsequent figures) in the S/D regions of the FinFET test structure. (b) Cross-sectional transmission electron microscopy image of the indicated S/D regions showing SiC:P growth on both the top and side surfaces of the fin, forming an extended Π-shaped S/D stressor that wraps around the Si fin for maximum lattice interaction.

the dependence of the epitaxial quality on the S/D recess shape is eliminated. To induce tensile channel stress in the FinFETs, the SiC:P process was optimized to selectively grow SiC:P films on the FinFET S/D regions. In Fig. 4(a), an isometric-view scanning electron microscopy (SEM) image shows the selective growth of SiC:P with 1.7 at.% of substitutional carbon concentration (also denoted as "SiC:P 1.7%" in this paper) in the S/D regions of a FinFET test structure. Details of the process used to achieve the selective SiC:P films can be found in [18]. The formation of gate spacers involved an extra *in situ* etch to remove the fin spacers, exposing the side surfaces of the fin for epitaxial growth, resulting in the formation of extended Π-shaped SiC:P S/D stressors, where the SiC:P epilayer fully covers the top and sidewall surfaces of the fin [Fig. 4(b)]. The wrapping of the S/D stressor around the Si fin ensures maximum lattice interaction for efficient lattice strain coupling from the S/D stressors to the channel. Since the SiC:P S/D stressors are *in situ* doped with phosphorus to a concentration of 3×10^{20} cm^{-3}, parasitic S/D series resistances are also effectively reduced. With *in situ* doping, an additional high-temperature spike anneal for dopant activation becomes unnecessary and is eliminated in the device fabrication process. This is not only beneficial for preventing loss of carbon substitutionality but will also be helpful in preventing effective oxide thickness increases in transistors with ultrathin oxides or high-κ gate dielectrics.

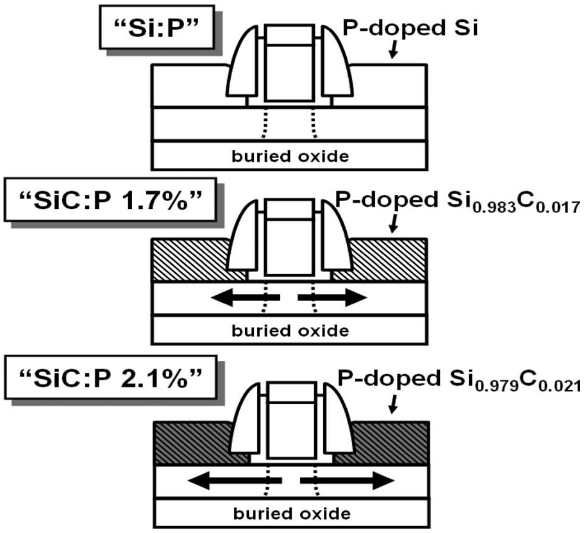

Fig. 5. Schematic showing the three splits fabricated in this paper. They are structurally similar, except for the selectively grown S/D epitaxial film. SiC:P with substitutional carbon percentages of 1.7% and 2.1% were grown in the S/D regions of the strained FinFETs. Si:P was grown in the S/D regions of the control FinFETs. The arrows indicate the strain directions.

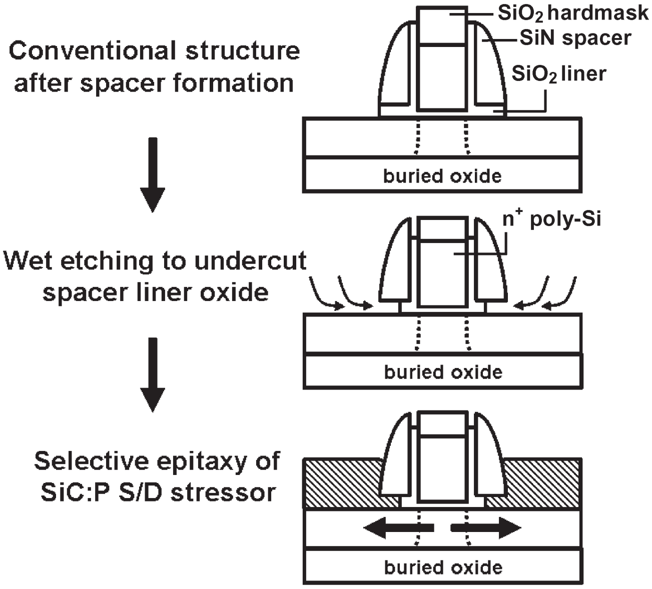

Fig. 6. Schematic showing the key steps for forming the SiC:P S/D stressors for strained devices or Si:P S/D for control devices. The arrows indicate the strain directions. Wet etching with HF is performed to undercut the SiO_2 liner oxide underneath the SiN spacers. This enables the epitaxial growth of SiC:P or Si:P in the SDE regions. Extension resistance is also reduced since the films are *in situ* doped. For FinFETs with SiC:P S/D, the closer proximity of S/D stressors to the channel leads to enhanced stress coupling for larger stress benefits.

Phosphorus-doped Si, $Si_{0.983}C_{0.017}$, and $Si_{0.979}C_{0.021}$ films were grown selectively in the S/D regions and are denoted as "Si:P," "SiC:P 1.7%," and "SiC:P 2.1%," respectively. A schematic depicting the device splits is shown in Fig. 5. All device splits undergo the same process steps up to the selective epitaxial growth of the raised S/D regions. As S/D epitaxial growth significantly reduces S/D series resistances [19], S/D epitaxial growth using Si:P was performed for the "Si:P" control devices to eliminate any S/D series resistance advantages that the "SiC:P" devices would otherwise have. Silicidation of the S/D regions was not performed in these experiments to maintain process simplicity. This avoids potential issues that would complicate the device analysis, such as additional silicide-induced stress effects [20] and differences in the silicidation properties of Si:P and SiC:P S/D regions with different substitutional carbon concentrations [21].

Undercutting of the spacer liner oxide was performed using wet etching with hydrofluoric acid (HF) prior to selective epitaxial growth of the S/D stressors. Fig. 6 illustrates how this simple process is done. Prior to epitaxial growth, a wet clean using dilute HF is typically performed to remove native oxide from the Si surface. By extending the duration of this HF cleaning step, it is possible to undercut the liner oxide underneath

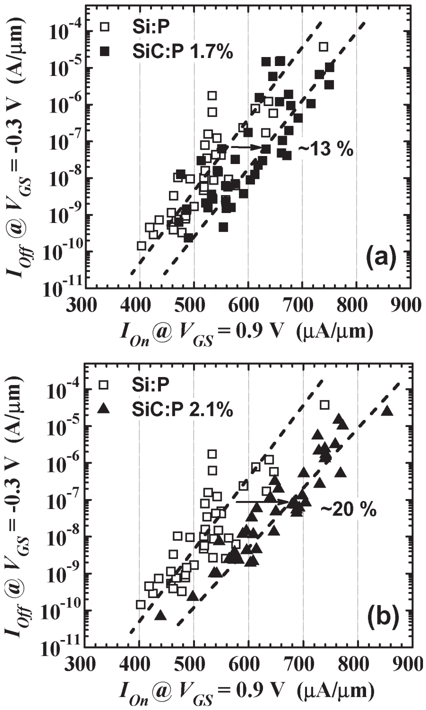

Fig. 7. (a) The $I_{\rm Off}$–$I_{\rm On}$ plot shows ∼13% enhancement in $I_{\rm On}$ at a fixed $I_{\rm Off}$ of 1×10^{-7} A/μm due to the incorporation of SiC:P S/D stressors with 1.7% substitutional carbon. (b) ∼20% enhancement in $I_{\rm On}$ is obtained for the devices with 2.1% substitutional carbon.

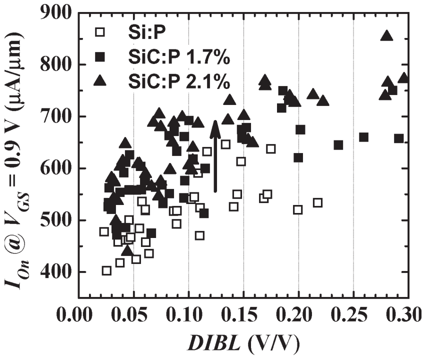

Fig. 8. Up to ∼20% enhancement in $I_{\rm On}$ can be obtained by incorporating SiC:P S/D stressors with 2.1% substitutional carbon at a fixed value of DIBL. For the split with SiC:P 1.7%, an enhancement of ∼15% can be obtained.

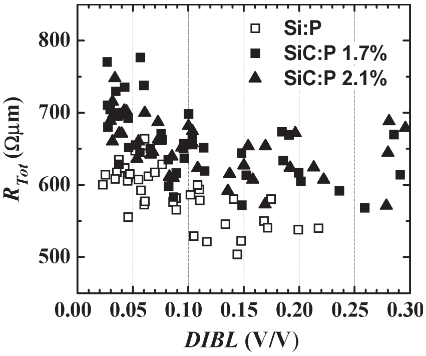

Fig. 9. Total resistance $R_{\rm Tot}$ at high gate overdrive is indicative of the S/D series resistances of the various types of devices ($R_{\rm Tot} = 50$ mV$/I_{\rm DS}$ at $V_{\rm GS} - V_{t,\rm lin} = 2.7$ V and $V_{\rm DS} = 50$ mV). It was found that Si:P devices have generally lower series resistances.

the nitride spacers. The degree of liner oxide undercut can be controlled by adjusting the duration of the HF cleaning step. This enables epitaxial growth not only on the exposed S/D regions outside of the gate nitride spacers but also underneath the gate nitride spacers. This effectively forms laterally encroached SiC:P S/D stressors for higher stress-coupling efficiency in the strained FinFETs. Furthermore, this also reduces the SDE resistances since the epitaxial films are *in situ* doped to a high doping concentration of 3×10^{20} cm^{-3} and have low sheet resistivity. In FinFETs or thin-body SOI FETs, where the SDE regions are very thin, SDE resistances can be a large fraction of the total parasitic series resistance. As such, reducing SDE resistances using laterally encroached *in situ* doped films can particularly be beneficial in such devices. It should, however, be noted that evaluation of the performance benefits of lateral stressor encroachment is not the focus of this paper.

IV. ELECTRICAL CHARACTERIZATION OF N-FinFETs WITH SiC:P S/D STRESSORS

$\langle 110\rangle$-oriented (110)-sidewall p-channel FinFETs tend to have good performance due to the high hole mobility of (110) surfaces. While $\langle 100\rangle$-oriented (100)-sidewall n-channel FinFETs tend to show better performance, $\langle 110\rangle$-oriented (110)-sidewall n-channel FinFETs can more densely be laid out beside similarly oriented p-channel counterparts, making them of particular importance in density critical applications, such as static RAM. All the devices discussed in this section are $\langle 110\rangle$-oriented (110)-sidewall n-channel DG FinFETs. The devices have gate lengths down to about 40 nm and fin widths of about 35 nm. Fig. 7(a) and (b) shows the $I_{\rm Off}$–$I_{\rm On}$ plots for FinFETs having SiC:P S/D with $C_{\rm sub}$ of 1.7% and 2.1%, respectively, compared to control FinFETs with *in situ* doped Si S/D (denoted as Si:P). At a fixed $I_{\rm Off}$ of 1×10^{-7} A/μm, Si:P, SiC:P 1.7%, and SiC:P 2.1% devices have an average $I_{\rm On}$ of 569, 642, and 681 μA/μm, respectively. FinFETs having SiC:P S/D stressors with $C_{\rm sub} = 1.7\%$ show ∼13% $I_{\rm On}$ enhancement at a fixed $I_{\rm Off}$ of 1×10^{-7} A/μm compared to the control. An excellent $I_{\rm On}$ enhancement of ∼20% over control was achieved for strained FinFETs with $C_{\rm sub} = 2.1\%$. This is a significant enhancement, considering that only 7% enhancement could be obtained in (110)-sidewall FinFETs with *non-in situ* doped $\rm Si_{0.99}C_{0.01}$ S/D stressors [6]. The performance enhancement is further confirmed by the $I_{\rm On}$ versus drain-induced barrier lowing (DIBL) plot in Fig. 8, which shows ∼15% and ∼20% enhancement for strained FinFETs with SiC:P S/D stressors having $C_{\rm sub}$ of 1.7% and 2.1% FinFETs, respectively, over the control FinFET with Si:P S/D at a DIBL of about 100 mV/V. As the DIBL is related to the effective channel length, comparing $I_{\rm On}$ enhancement at the same value of the DIBL illustrates the enhancement at the same effective channel length.

For a qualitative comparison of S/D series resistance, the total resistance ($R_{\rm Tot}$) at high gate overdrive was plotted against the DIBL (Fig. 9), where $R_{\rm Tot} = 50\,{\rm mV}/I_{\rm DS}$ at ($V_{\rm GS} - V_{t,\rm lin}) = 2.7$ V and $V_{\rm DS} = 50$ mV. At high values of gate overdrive, the value of the total resistance tends asymptotically toward the value of the S/D series resistance. This is because

TABLE I
SUMMARY OF DRIVE CURRENT AND TOTAL RESISTANCE VALUES

	Si:P	*SiC:P (1.7%)*	*SiC:P (2.1%)*
Median I_{On} (µA/µm), for I_{Off} between 1 x 10^{-7} to 1 x 10^{-8} A/µm	541	622	667
$\Delta I_{On} / I_{On, Si:P}$ (%), for I_{Off} between 1 x 10^{-7} to 1 x 10^{-8} A/µm	0	+15	+23
Median I_{On} (µA/µm), for DIBL between 0.07 to 0.15 V/V	537	618	650
$\Delta I_{On} / I_{On, Si:P}$ (%), for DIBL between 0.07 to 0.15 V/V	0	+15	+21
Median R_{Tot} (Ωµm), for DIBL between 0.07 to 0.15 V/V	578	644	655
$\Delta R_{Tot} / R_{Tot, Si:P}$ (%), for DIBL between 0.07 to 0.15 V/V	0	+11	+13

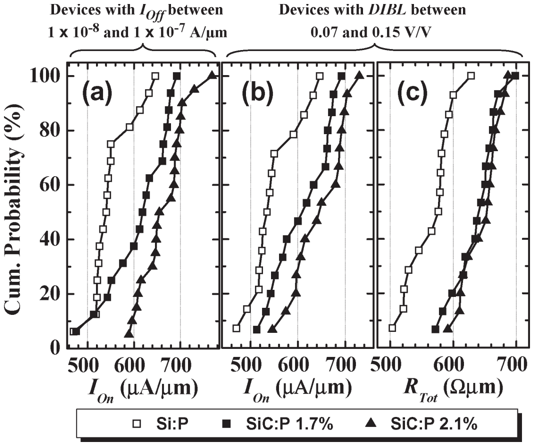

Fig. 10. Cumulative distributions of the (a) $I_{\rm On}$ of devices with $I_{\rm Off}$ between 1×10^{-8} and 1×10^{-7} A/μm and the (b) $I_{\rm On}$ and (c) $R_{\rm Tot}$ of devices with DIBL between 0.07 and 0.15 V/V.

the channel resistance decreases with increasing gate overdrive (and decreasing effective channel length), whereas the S/D series resistance stays relatively constant, approximating an asymptotic behavior in which $R_{\rm Tot}$ tends toward the value of S/D series resistance at high gate overdrive. This allows for a qualitative comparison of the S/D series resistances using $R_{\rm Tot}$. It is clearly observed that the FinFETs with Si:P S/D have lower S/D series resistances than the FinFETs with SiC:P S/D stressors. This can be attributed to the greater S/D series resistance reduction in FinFETs with Si:P S/D compared to the FinFETs with SiC:P S/D stressors. This is due to the lower resistivity in the Si:P films compared to the SiC:P films. Sheet resistance measurements confirm this, as sheet resistances of 75, 128, and 160 Ω/sq were obtained for Si:P, SiC:P 1.7%, and SiC:P 2.1%, respectively. This implies that the actual strained-induced enhancement could possibly be larger but is somewhat suppressed by the influence of larger S/D parasitic resistances in the devices with SiC:P S/D.

The data points in Figs. 7–9 show some degree of spread due to the inherent variability of the fabricated devices. The overlap of some data points may make it difficult to discern the quantitative differences in the values. In order to give a statistical summary of the data, the cumulative distributions of $I_{\rm On}$ for devices with values of $I_{\rm Off}$ between 1×10^{-8} and 1×10^{-7} A/μm [Fig. 10(a)] and $I_{\rm On}$ [Fig. 10(b)] and $R_{\rm Tot}$ [Fig. 10(c)] for devices with values of DIBL between 0.07 and 0.15 V/V are plotted in Fig. 10. Table I summarizes the median values obtained from Fig. 10, which is less dependent on the values of outliers, and thus provides a more accurate representation of the data. Overall, an $I_{\rm On}$ enhancement of 15% and 21%–23% can be obtained by incorporating S/D stressors comprising SiC:P (1.7%) and SiC:P (2.1%). On the other hand, the increase in $R_{\rm Tot}$ by 11% and 13%, as discussed earlier, indicates the increase in the S/D series resistances of the SiC:P devices. Hence, Table I clearly shows that significant $I_{\rm On}$ enhancement can still be obtained in spite of the slight increases in S/D series resistances. The application of an optimized S/D silicidation scheme is expected to reduce the differences in the S/D series resistances.

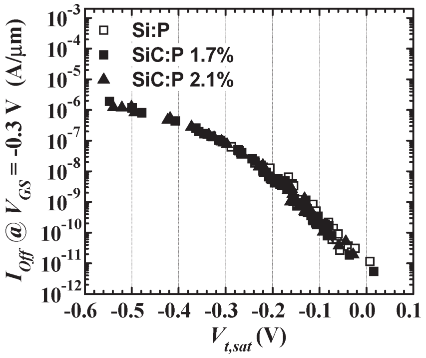

Fig. 11. Excellent match in the control of short-channel effects for both Si:P and SiC:P devices is evident from the comparable $I_{\rm Off}$ for devices with different values of $V_{t,{\rm sat}}$. The threshold voltage is lower than usual due to the use of n$^+$ poly-Si gate with a relatively low channel doping concentration.

Next, we evaluate the short-channel matching of SiC:P S/D FinFETs compared with Si:P S/D FinFETs. Fig. 11 plots $I_{\rm Off}$ against $V_{t,{\rm sat}}$ for the devices from all three splits. The comparable $I_{\rm Off}$ at various values of $V_{t,{\rm sat}}$ indicates excellent matching in short-channel control. This confirms that the epitaxial processes for SiC:P did not degrade the short-channel effects of the devices. This is expected since the epitaxial processes employed a very low thermal budget. Instead, high growth rates at low epitaxial growth temperatures were ensured by adopting appropriate growth precursors. Fig. 12(a) and (b) plots the cumulative distributions of the subthreshold swing (SS) and DIBL of the devices shown in the $I_{\rm Off}$–$I_{\rm On}$ plots. The relatively large spread in the data points is due to the fact that the devices that comprise the $I_{\rm Off}$–$I_{\rm On}$ plots have a variety of

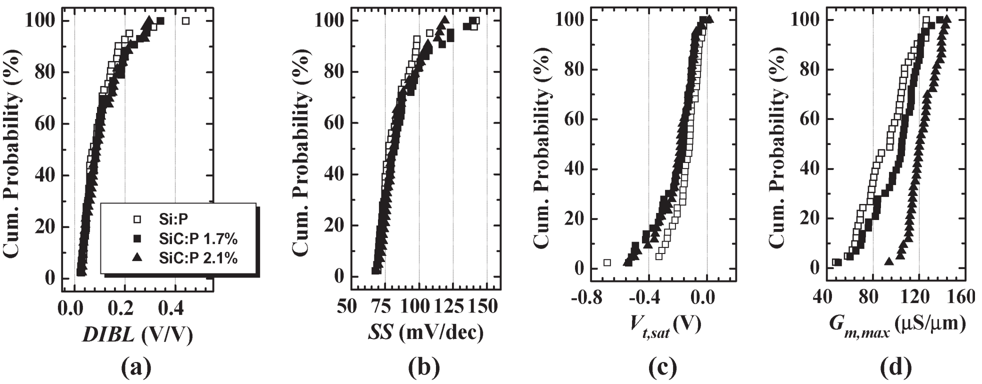

Fig. 12. Cumulative distributions of the (a) DIBL, (b) SS, (c) $V_{t,\mathrm{sat}}$ ($V_{t,\mathrm{sat}} = V_{\mathrm{GS}}$ at $I_{\mathrm{DS}} = 1\ \mu\mathrm{A}/\mu\mathrm{m}$ and $V_{\mathrm{DS}} = 1.2$ V), and (d) $G_{m,\max}$ of all the FinFET devices employed in the I_{Off}–I_{On} plots. All three splits have comparable SS and DIBL, suggesting similar short-channel control in devices from all three splits. $V_{t,\mathrm{sat}}$ is lower for the strained devices than that for the control, possibly due to strain-induced conduction band lowering. The $G_{m,\max}$ of both SiC:P splits show enhancement over the Si:P control.

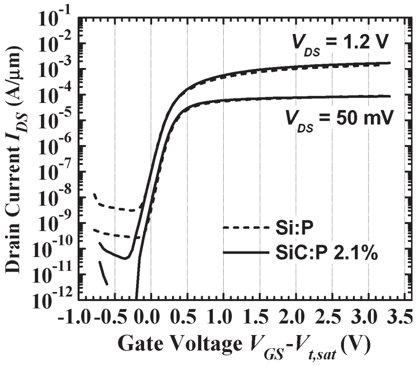

Fig. 13. Transfer characteristics of a pair of matched FinFET devices showing comparable DIBL and SS. The DIBL is 85 mV/V, and the SS is 80 mV/dec ($V_{t,\mathrm{sat}} = V_{\mathrm{GS}}$ at $I_{\mathrm{DS}} = 100\ \mathrm{nA}/\mu\mathrm{m}$ and $V_{\mathrm{DS}} = 1.2$ V).

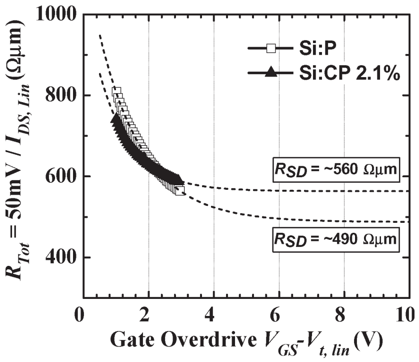

Fig. 14. S/D series resistances of the matched devices were estimated by extrapolating R_{Tot} to high gate overdrive voltages using a first-order exponential decay fit. The Si:P device has a slightly lower series resistance than the SiC:P 2.1% device.

gate lengths. Nevertheless, all three splits show comparable SS and DIBL, which, once again, points toward excellent short-channel matching between Si:P and SiC:P devices. Fig. 12(c) shows the cumulative distribution of $V_{t,\mathrm{sat}}$. The slight decrease in threshold voltage can be attributed to channel strain-induced conduction band lowering. Fig. 12(d) shows a clear enhancement in the peak transconductance $G_{m,\max}$ of the SiC:P devices over that of the Si:P devices. $G_{m,\max}$ enhancement is often attributed to mobility enhancement in strained transistors due to its reduced dependence on the S/D series resistance effects. Hence, the enhancement in $G_{m,\max}$ gives further evidence for the strain-induced mobility enhancement.

A matched pair of SiC:P 2.1% and Si:P FinFETs were examined more closely. Fig. 13 shows the I_D–V_G transfer characteristics of the matched pair. Both these devices have a DIBL value of ~85 mV/V and an SS of ~80 mV/dec, indicating that they have approximately the same effective channel length. To further ensure a fair comparison, the S/D series resistances of the devices were estimated and compared. R_{Tot} is plotted against gate overdrive in Fig. 14. A first-order exponential decay fit of the data points was performed to extract the R_{SD} values of the devices [22]. While this method of R_{SD} extraction may not possess the best absolute accuracy, it provides for a good qualitative comparison for single devices in nanoscale multiple-gate FETs, where device-to-device fluctuation can be larger that that of their planar counterparts. The series resistance of the Si:P device ($\sim 490\ \Omega\mu\mathrm{m}$) was extracted to be slightly lower than that of the strained SiC:P 2.1% device ($\sim 560\ \Omega\mu\mathrm{m}$). This difference in the series resistance is attributed to the difference in resistivity of the laterally encroached regions of the Si:P and SiC:P. Fig. 15 plots the I_D–V_D family of curves for the same devices. It shows that incorporating SiC:P S/D stressors with $C_{\mathrm{sub}} = 2.1\%$ gives a ~23% enhancement for this particular device over the Si:P control, despite the fact that the series resistance difference is in favor of the Si:P device.

V. CONCLUSION

The effectiveness of *in situ* doped high-substitutional-carbon SiC:P S/D stressors in enhancing I_{Dsat} for $\langle 110\rangle$-oriented (110)-sidewall DG FinFETs has been explored. It was found that a significant 20% strain-induced enhancement was obtained in SiC:P S/D FinFETs, incorporating a substitutional carbon concentration of 2.1%. This culminated in an I_{Dsat} value of 716 $\mu\mathrm{A}/\mu\mathrm{m}$, which is quite high, particularly when considering that the S/D regions were not silicided.

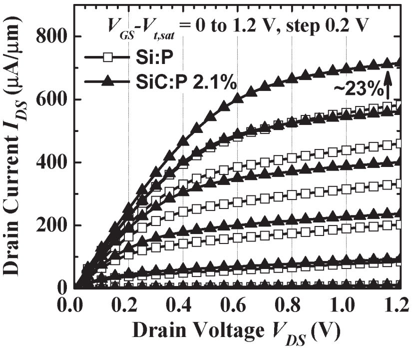

Fig. 15. $I_{\rm DS}$–$V_{\rm DS}$ curves showing 23% $I_{\rm Dsat}$ enhancement for this pair of matched devices ($V_{t,\rm sat} = V_{\rm GS}$ at $I_{\rm DS} = 100$ nA/μm and $V_{\rm DS} = 1.2$ V). This enhancement is mainly attributed to strain effects.

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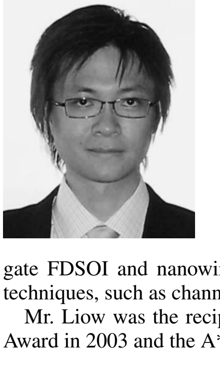

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