EPRC – 9 Project Proposal

TSV Technology for Packaging of Cu Low K Chip

24 August 2007

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Introduction

Background

- **Cu low-K technology is moving towards finer feature and newer Low K materials**
  - 90nm → 65nm → 45nm technology with Cu-low K → Ultra low K materials
  - Higher performance chip require higher I/O, finer pitch, larger chip size
  - Bottle neck: Feature size of build up substrate can not keep pace with device trend
  - Concern: Assembly, materials and reliability impact on the 45nm Cu / Ultra low K chip is not well understood
  - A solution to realize low stress packaging and high density interconnection is needed
- **IME has capabilities in related technologies**
  - Cu low K packaging with 150um bump pitch, Pb free solder and organic BU substrate
  - Core competencies in Thru-Silicon-Via (TSV) technology
  - Package design for high performance application

Motivation

- Si carrier with TSV technology is emerging solution for high performance integration platform for SiP technology
- TSV chip stacking is potential solution to minimize Chip-Packaging performance gap, allowing chip-chip high I/O interconnection, and minimizing CTE thermal-mechanical mismatch / low stress solution for large die Cu/Ultra Low K chip.

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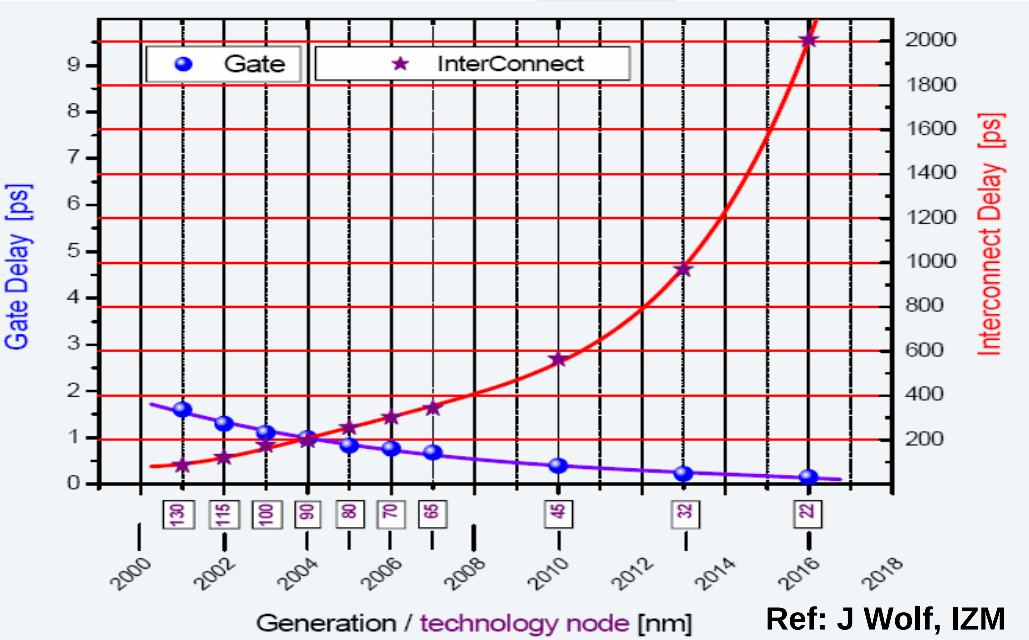
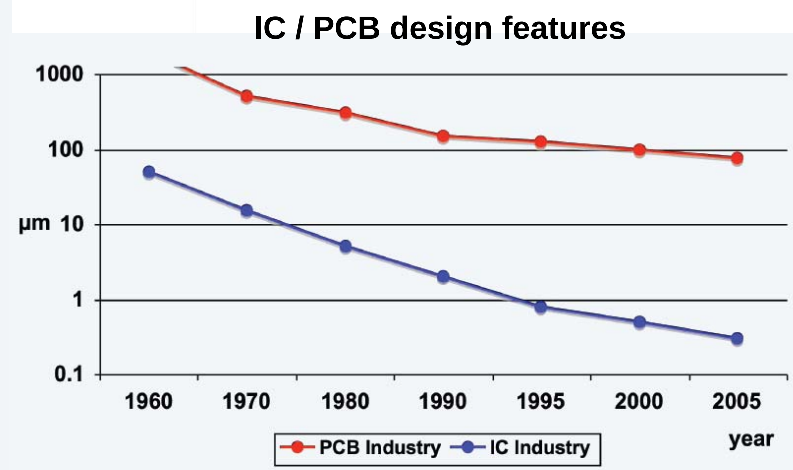
Chip – Package Performance & Technology Gap



Ref: J Wolf, IZM

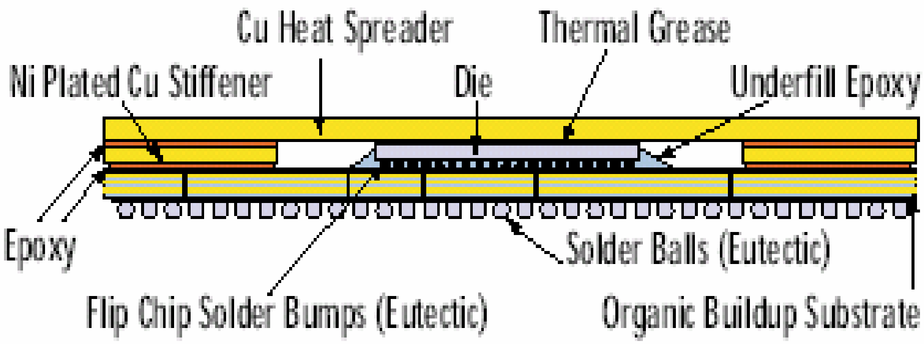


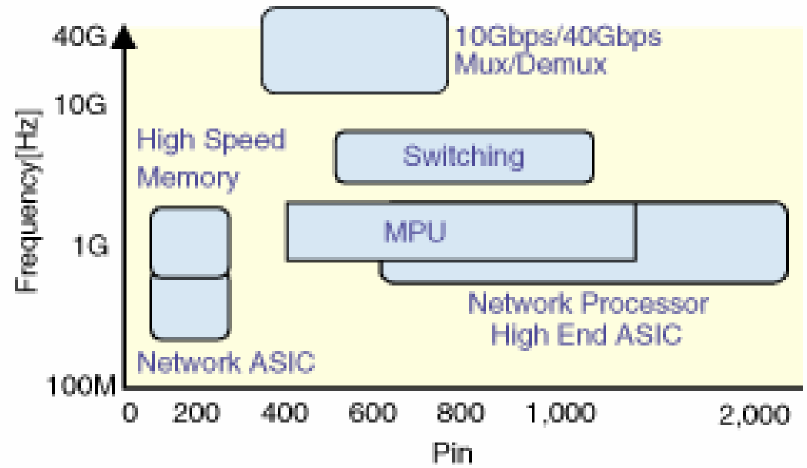
Ref; Gottward, EIPC

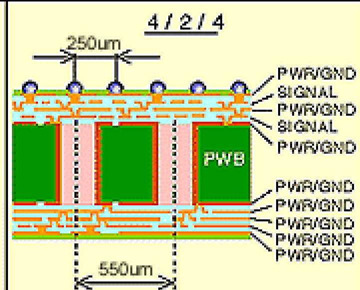
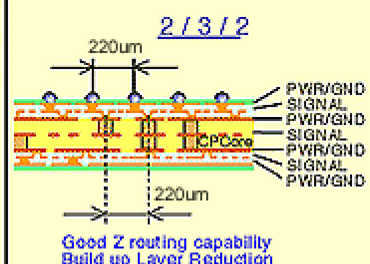
	2005	2006	2007	2008	2009
Cu low K technology (nm)	90	65	65	45	45
Chip size (high performance) (mm^2)	600 (~24x24)	630 (~25x25)	662 (~26x26)	695 (~26x26)	729 (~27x27)
Performance On-chip/off-chip (GHz)	5.2/3.1	5.7/3.9	6.8/4.9	8.1/6.1	9.8/7.6
Bump pitch (um)	150	130	130	130	120
Power density (Watt/mm2)	0.54	0.58	0.61	0.64	0.64

Ref: ITRS 2006

FCBGA using build-up substrates

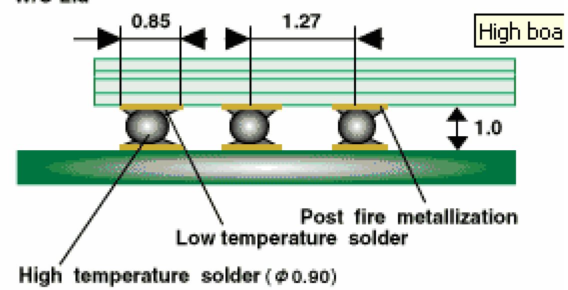




		HDBU	SHDBU
Typical Structure			
Core	Via Structure	Through Hole	Stacked Via
	Via Pitch	550	220

	HITCE	FR-4 (MCL-E-67)	ALUMINA
T.C.E	12.3	13~16	7.0
CONDUCTOR	Cu base	Cu	W
Dielectric Constant	5.3	4.5~4.8	10

Package : 50mmSQ / 1.2mmt,1.8mmt
PWB : 65mmSQ /1.6mmt / FR-4
W/O Lid



Ref: www.global.kyocera.com

- **Organic build up substrate has concern on fine pitch requirements. Advanced BU substrate is getting more costly.**
- **Alternative solution of using ceramic substrate is not attractive due to high cost and fine pitch limitation.**

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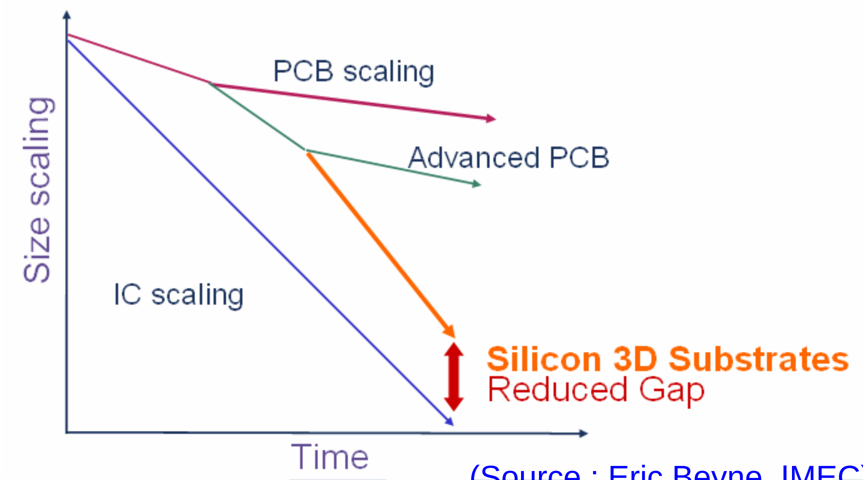
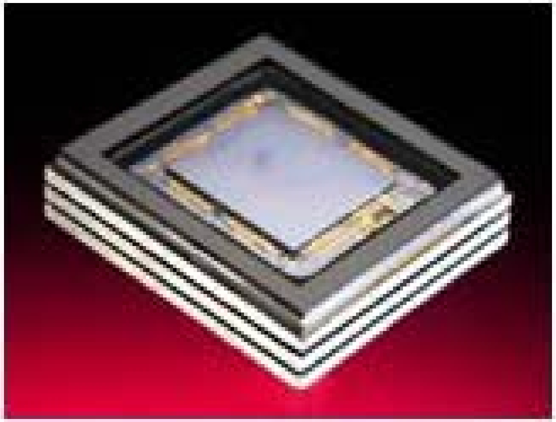
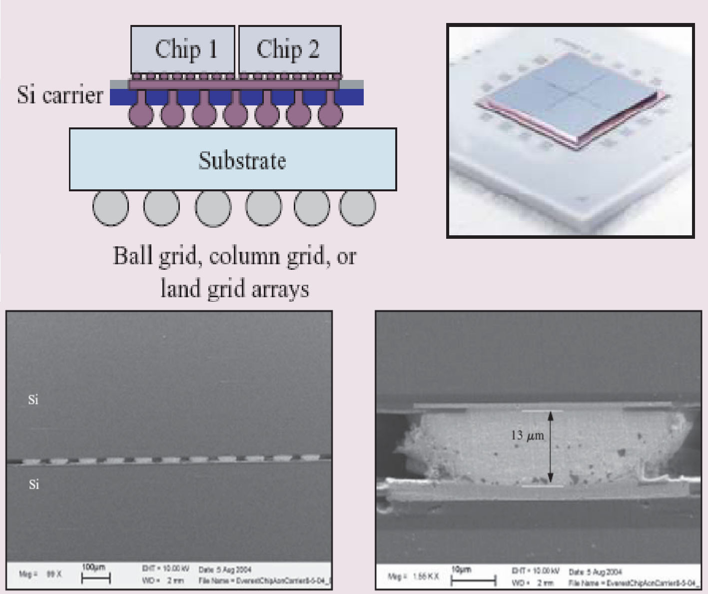
Packaging with Si carrier & TSV



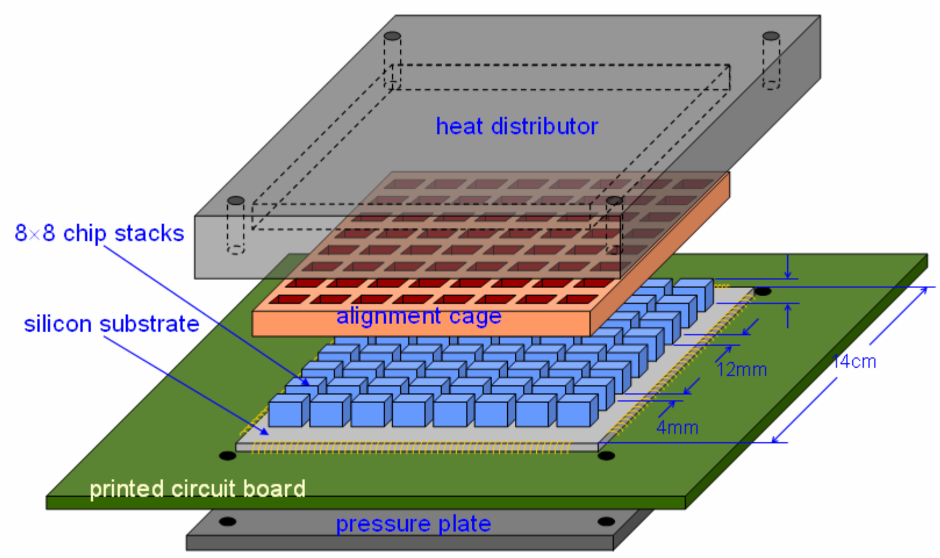
(Source : Eric Beyne, IMEC)



Source: IME's Si stacked module (2005)



(Ref : Knickerbocker, IBM J. Res & Dev, 2005)



(Source : Intel, US)

Silicon carrier with TSV is emerging solution for high performance integration platform

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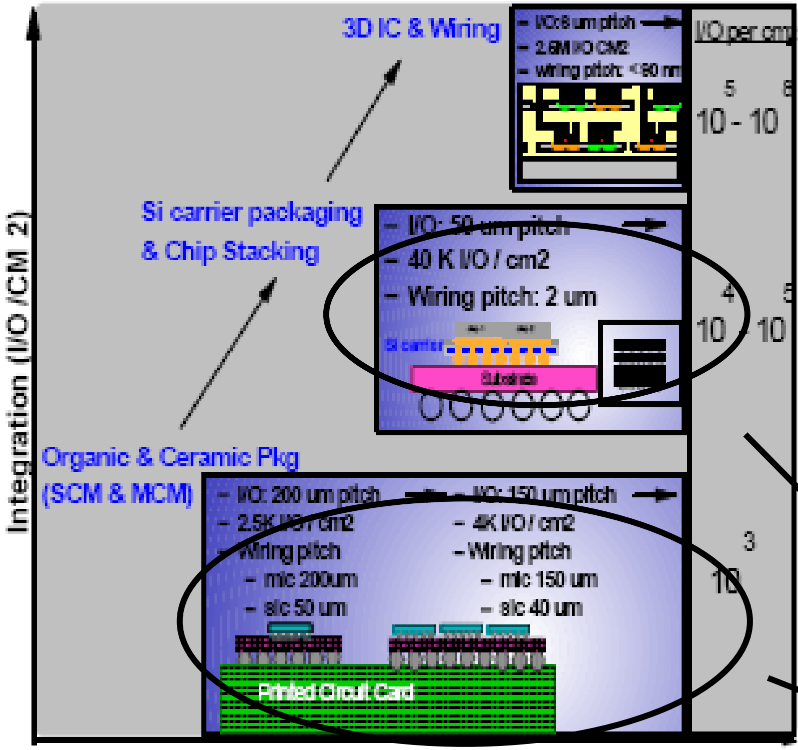
High Density Packaging Trend – TSV chip carrier



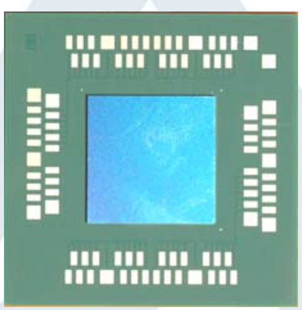
(Source : IBM)

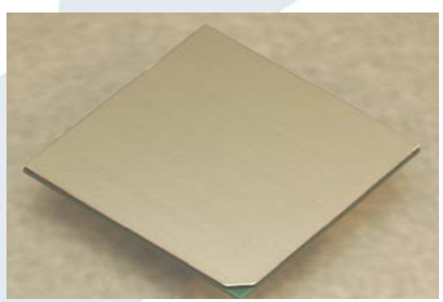
EPRC 9

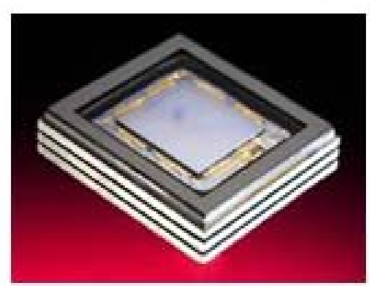
EPRC 7 & 8

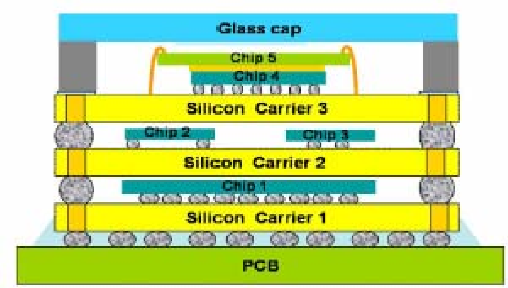
Advantages

- High density interconnect
  - Huge gap between front end scaling, interconnect pitch & substrate scaling
- Absence of thermal mismatch, so micro-flip chip interconnection
- Good thermal conductivity
- Thin film process for embedded passives









Schematics of Stacking Concept

Ref: IME's FCBGA and Stack chip module developed in EPRC 7 & 8

- Silicon carrier can realize many advantages using its well established design & process technologies
- IME has developed TSV related technologies since 2005

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Proposed Project:
TSV Technology for Packaging of Cu Low K Chip

Objective:

To develop TSV technology for Cu/Low K chip with very fine pitch interconnection involving:

- Electrical design of Si interposer and a simplified organic substrate aiming for Cu/Ultra Low K chip application
- Evaluation of TSV technology and develop processes for the Si interposer
- Physical design, fabrication, assembly and reliability assessment

Scope:

- Electrical design and characterization of TSV interposer for FCBGA application
- Mechanical design, modeling and optimization
- TSV interposer process evaluation and fabrication
- Assembly process evaluation, including fine pitch interconnection, under fill / flux material characterization and selection, wafer backgrind and dicing
- Reliability assessment and failure analysis

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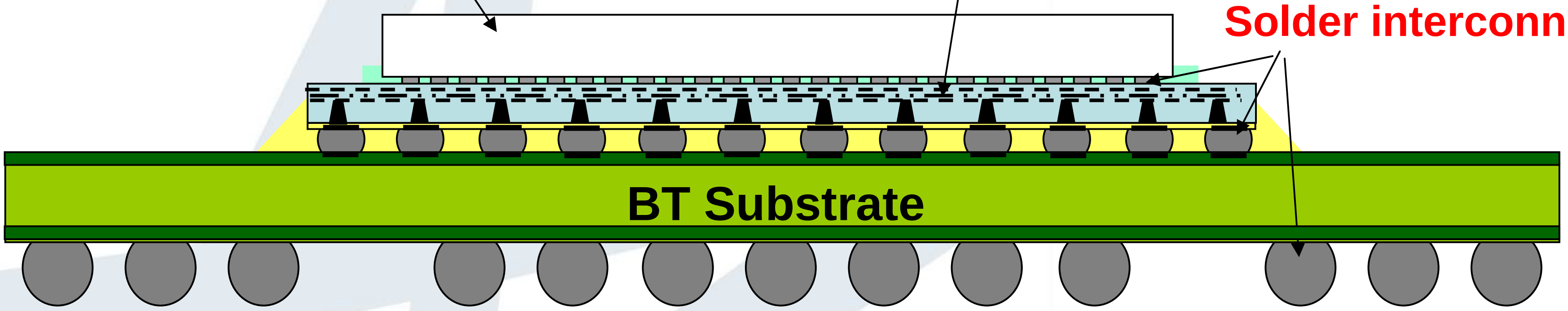
Proposed Test Vehicle (Option 1)



Features:

Die size:	>= 20x20mm*
Chip technology:	Cu/low K*
Cu low K bump pitch:	150 um*
Micro bump type	solder
TSV interposer bump pitch:	<= 250um
BT substrate ball pitch:	1 mm
Substrate solder & materials:	RoHS compliant solders and materials

(Remark * subjected to availability)

Advantages

- High density interconnection
- Minimum CTE mismatch
- Reliability for Cu Ultra Low K chip
- Less constraint on underfill
- Micro flip chip interconnection
- Low cost BT substrate

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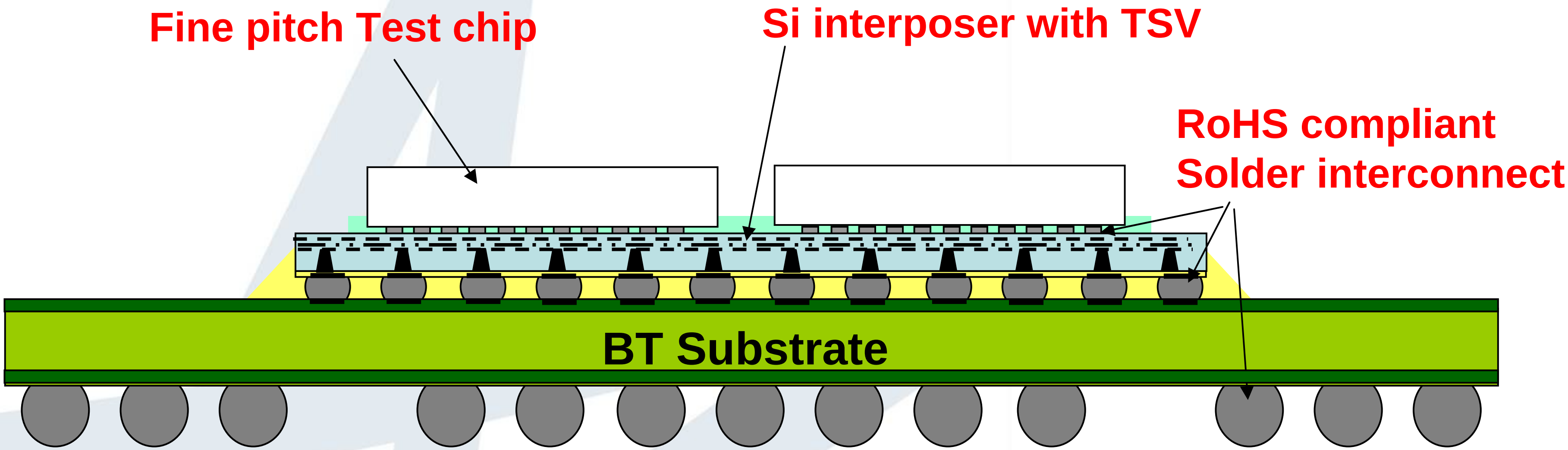
Proposed Test Vehicle (Option 2)



Features:

Die size:	>= 2x10x12mm*
Chip technology:	Cu/low K* or Al Test chip
Bump pitch:	50, 100, 150 um
Micro bump type	solder, Cu, Au
TSV interposer bump pitch:	<= 250um
BT substrate ball pitch:	1 mm
Substrate solder & materials:	RoHS compliant solders and materials

(Remark * subjected to availability)

Advantages

- High density interconnection
- Minimum CTE mismatch
- Reliability for Cu Ultra Low K chip
- Less constraint on underfill
- Micro flip chip interconnection
- Low cost BT substrate

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Key Challenges

- **Packaging design**
  - Electrical design & characterization for Si interposer
    - High speed interconnect / via design
    - Power distribution network design and optimization
  - Structural design and optimization
    - Stress analysis of detailed low K / ultra low K / Si interposer structures under assembly and reliability condition
    - Package / Si interposer design optimization
- **TSV interposer technology**
  - Dielectric isolation process
  - High speed via architectures
  - Via filling method
  - Thin wafer support
- **Assembly, materials, and reliability**
  - Underfill, flux material selection
  - Wafer backgrinding and dicing (Cu low k bumped wafer & Silicon carrier)
  - Micro-bump interconnection and assembly processes
  - Reliability and FA

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Project Deliverables

- Design guidelines of using Si interposer with simplified organic substrate for FCBGA application
- Electrical modeling results and characterization data for Si interposer with TSV
- Mechanical & thermal modeling results and optimization
- Process details of Si interposer with TSV
- Micro-bump interconnection assembly characterization
- Large die Cu low K assembly processes, including under fill, flux characterization and selection
- Reliability assessment results and failure analysis

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