

EPRC – 9 Project Proposal

Embedded Micro Wafer level Packaging

24 August 2007

Trends : Embedded Technology

Ubiquitous Computing

Automatic order system
RFID, USN(Uniquest Sensor Network)

Wearable Electronics –
Miniaturized Powerful Portable PC available / ultra-fast wireless internet connection / Various sensor systems (health monitoring)

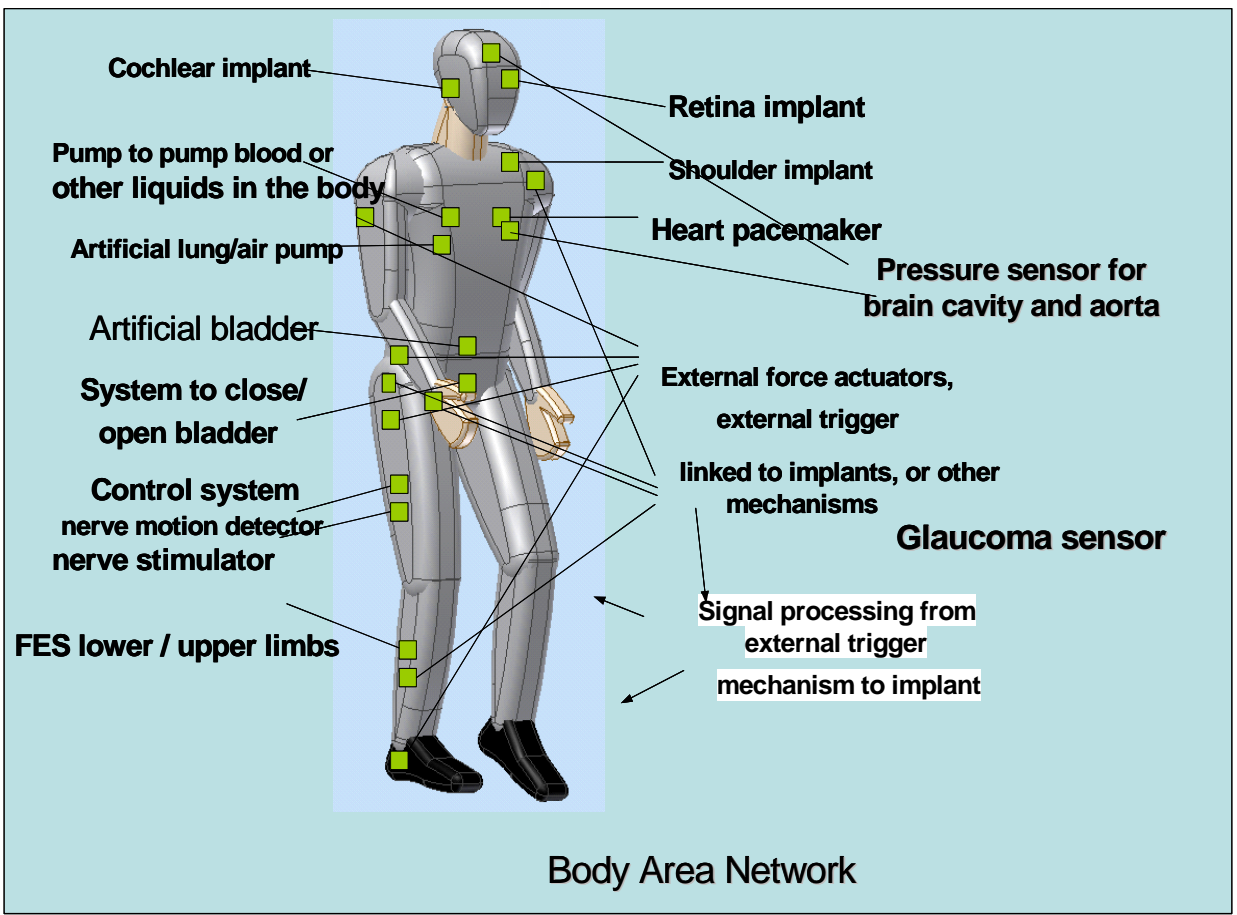
Internet Mobile Education System
E-learning
M-learning

Multimedia broadcasting
(TV, movie etc.)
DMB, VOD

Watch including database storage / weather forecasting (with connection to server)

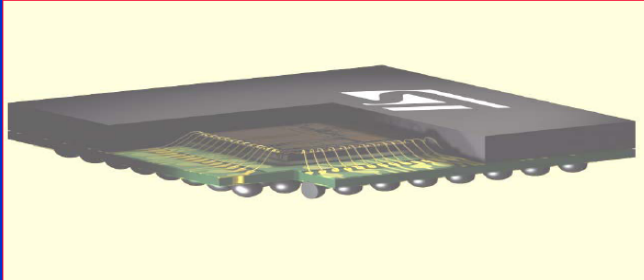
Foldable Display-news paper/magazine (e-book, e-ink, WiBro)

Auto-Navigation System/GPS services
(Telematics, LBS)



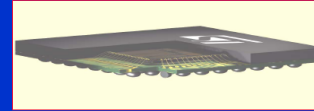
(Source : Samsung)

Technology Trends- BGA & FBGA Packages



Ball Grid Array (BGA)
Ideal for Multiple Interconnections inside the Package:
Single Chip, Multichip,
System in Package (Like a “plastic hybrid”)

10% of total volume; 100% of advanced applications



Ball Grid Array (BGA) Market (2007)

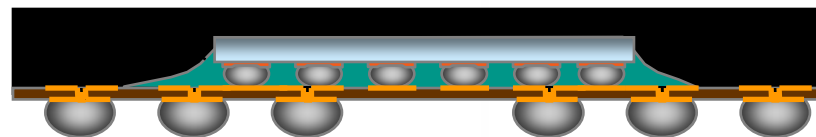
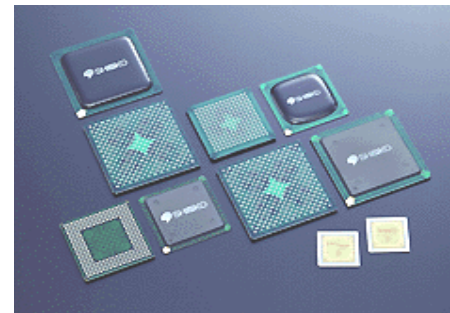
	Small CSP / BGA (ASICs, memories)	Large PBGA (micro, graphics)
Volume (bn units)	8	2
Area (sq m)	1 million	2 million
# layers	2-6	2-12
Yield (%)	90 - 95	70 - 90
Panel size (mm)	400 x 500	300 x 400
Panel Mkt Price (\$)	50 - 350	\$\$\$
Total Value (bn\$)	1.0 - 1.5	5

DRIVER TO INTEGRATION / MINIATURIZATION: MOBILE PHONE






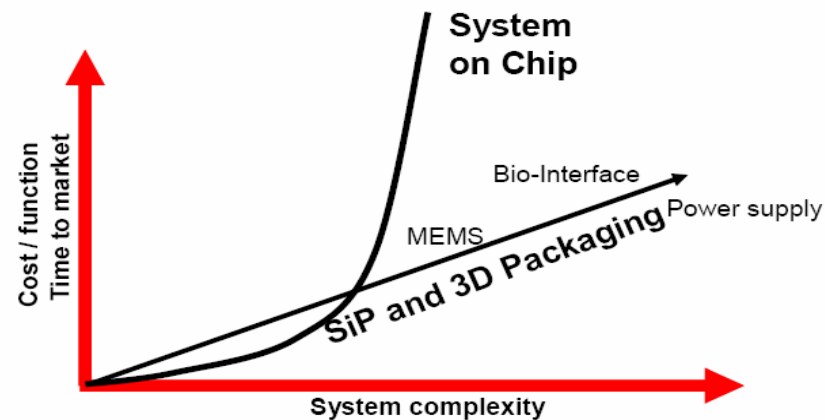
- 1bn Units / year
- 800 to 1200 components/ unit
- 8 to 12 layer motherboard (cost)
- shielding (cost)

It changes the conventional idea of packaging : 2D is not enough



Trends : SiP Integration

Chip / Component Configuration	Technology
Side by Side Placement	<p>Substrate: organic laminate, ceramic, glas, silicon, leadframe</p> <p>Chip interconnection: wire bond and/or flip chip</p> <p>+ passive components</p> <p>integrated into the substrate discrete (CSP, SMD)</p> 
Stacked Structure	<p>PoP PIP</p> <p>stacked die — wire bond, WB +FC</p> <p>chip to chip / wafer</p> <p>flip chip, face to face through silicon</p> <p>WL 3D stack</p> <p>wafer to wafer (W2W)</p> 
Embedded Structure	<p>Chip in PCB / polymer — single layer multi-layer 3D stack</p> <p>WL thin chip integration — single layer stacked functional layers</p> 



(Source : ITRS Roadmap 2007)

SoC and SiP Comparison for Cost per Function and Time to Market vs. Complexity

Technology Trends: Embedded Wafer Level Level Packaging

100% size

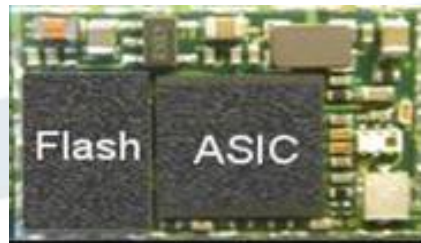
24.5 x 14.5 mm



Substrate: FR4

75% size

19.9 x 13.3 mm



Substrate: FR4

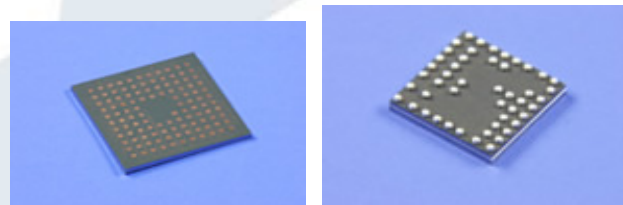
28% size

10.0 x 10.0 mm



ASIC
+
Flash

Substrate: LTCC BGA,
7 Layers ,
0201 Chips



14% size

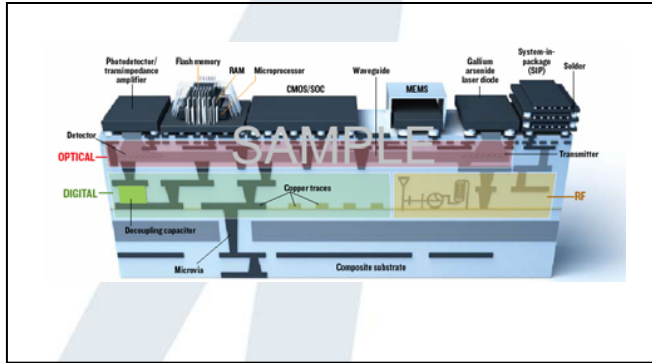
6.5 x 6.5 mm

Substrate: Nil

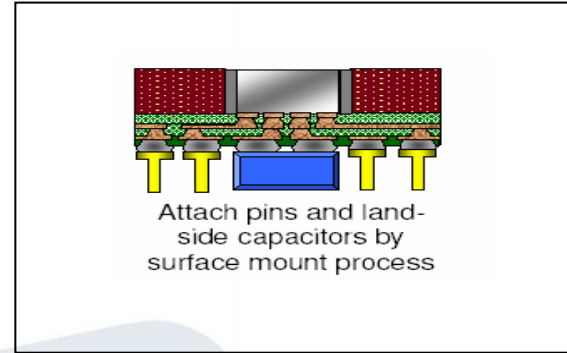
Embedded Technology

(Source : Casio)

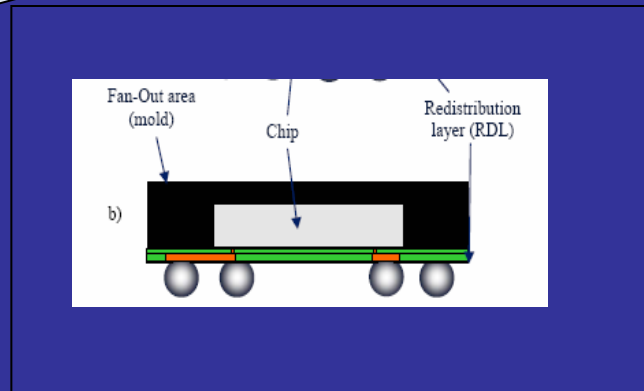
Methods of Embedding



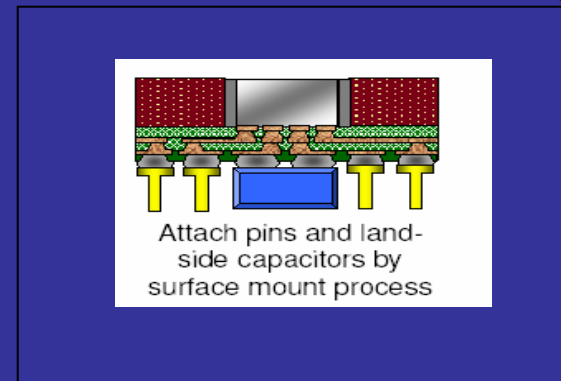
Embedding into PC Boards



Embedding in Package



Wafer Level Process based



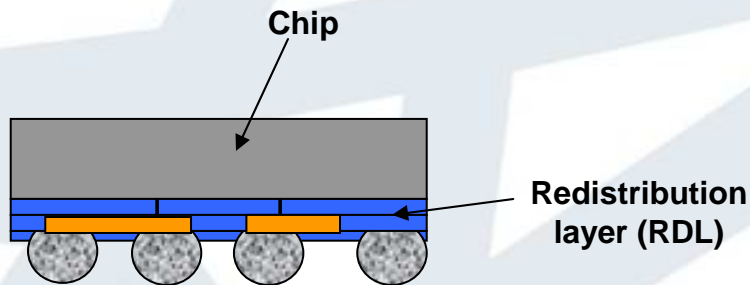
Laminate Based

(Source : Intel, Infineon & GaTech)

Challenges with conventional Wafer level packaging

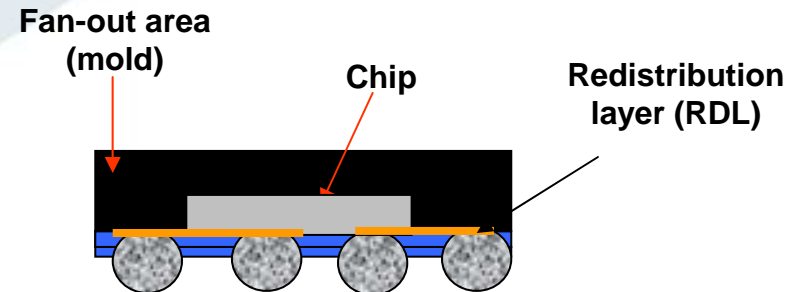
Technology Trends:

- High density integration
- Low profile package
- Embedding actives and passives
- System level integration – Possibilities of MEMS, Optical and hybrid integration – More multi chip packaging requirements



Conventional WLP

- Fan In Interconnects only
- Silicon lossy substrate for passives and RDL
- Only Single chip packaging solution
- Wafer Level Yield issues



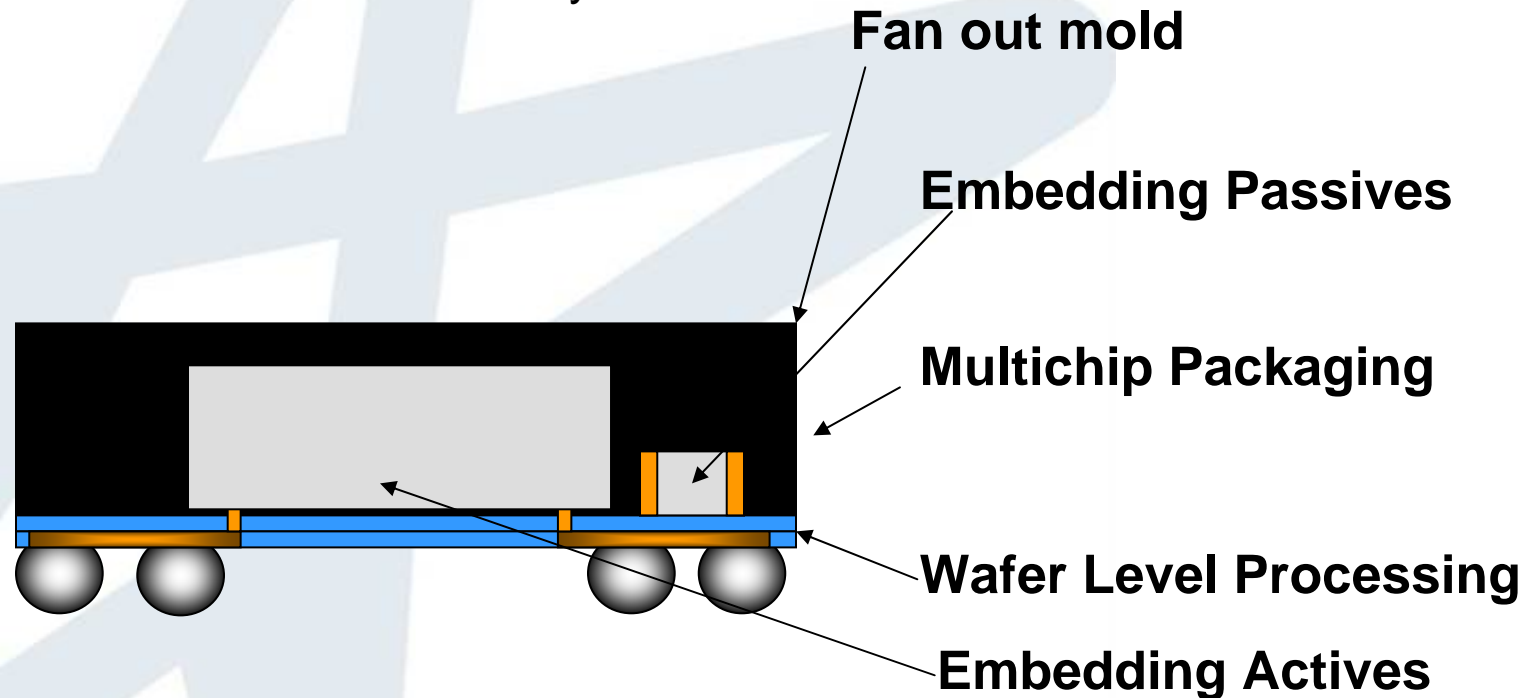
Embedded Micro WLP

- Fan out Interconnects
- Best of Silicon and Best of polymer for passives and RDL
- Single/Multi chip packaging solution
- Better Wafer Level Yield
- Embedding of Chip passives

Embedded Packaging Technology

Motivation

- Wafer level packaging approaches are strongly demanded by the industry for miniaturization and low cost application such as hand held and PAN device applications.
- Conventional wafer level packaging has issue due to fan in interconnect, lossy silicon substrate and wafer level yield.



Embedding Actives and passives in substrate and packages is key technology for product miniaturization. 20-60 parts /cm² is looked in future products

- Panel Discussion ECTC 2006

Proposed Project: Embedded Micro Wafer level Packaging

Objective:

To develop embedded wafer level packaging solution simultaneously achieving

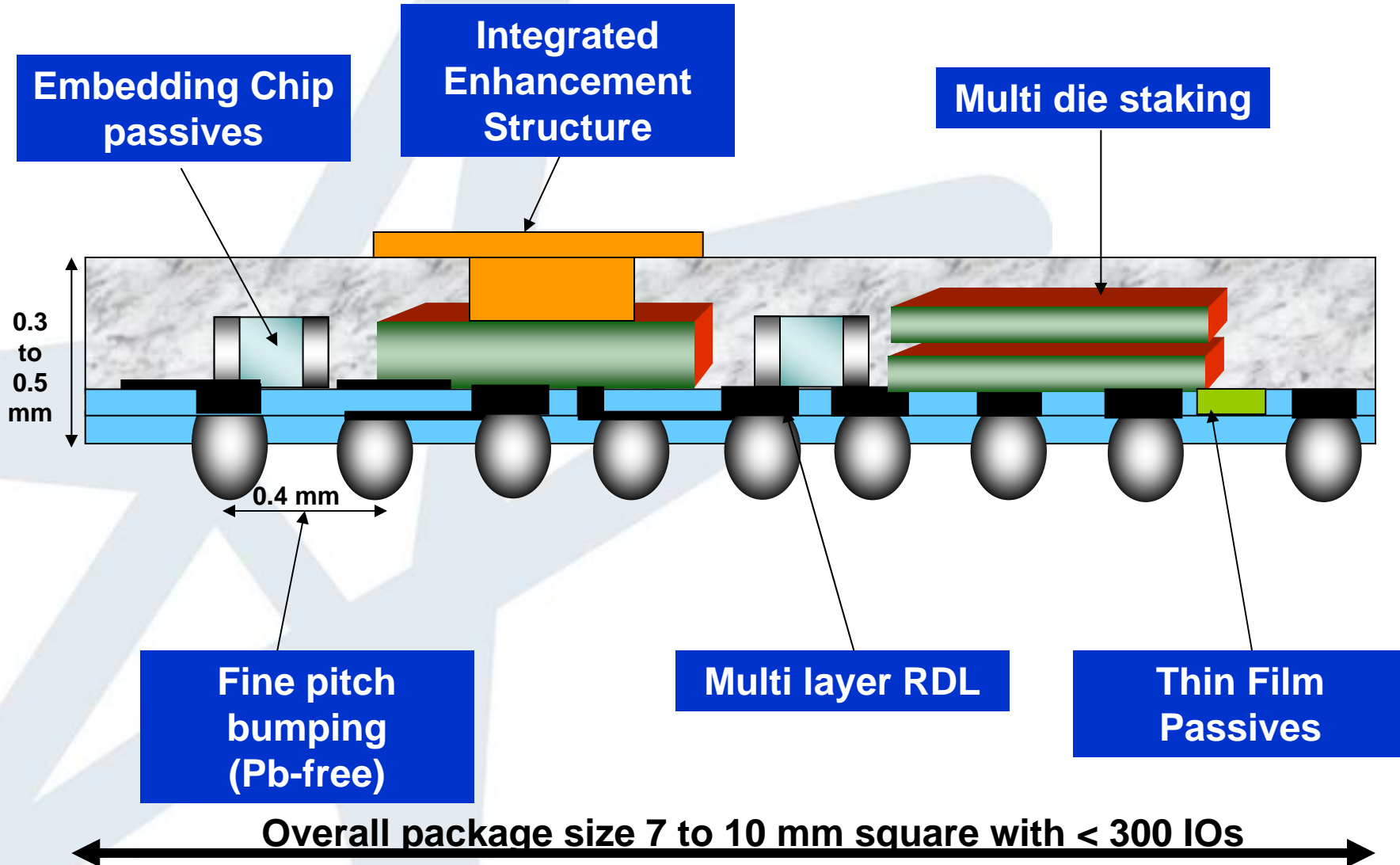
- Wafer level reconstruction of multiple chip using fan out interconnects
- Embedding passives design and fabrication
- Assessment of Electrical and reliability performance

Scope:

- Mechanical modeling & optimization of package structure
- Electrical modeling and design guide lines for embedded passives and signal integrity
- Process development for wafer level reconstruction of multiple chip and multilayer RDL
- Integrated enhancement structures such as Thermal, Antenna, EMI shield
- Wafer level molding process and optimization
- Reliability performance assessment

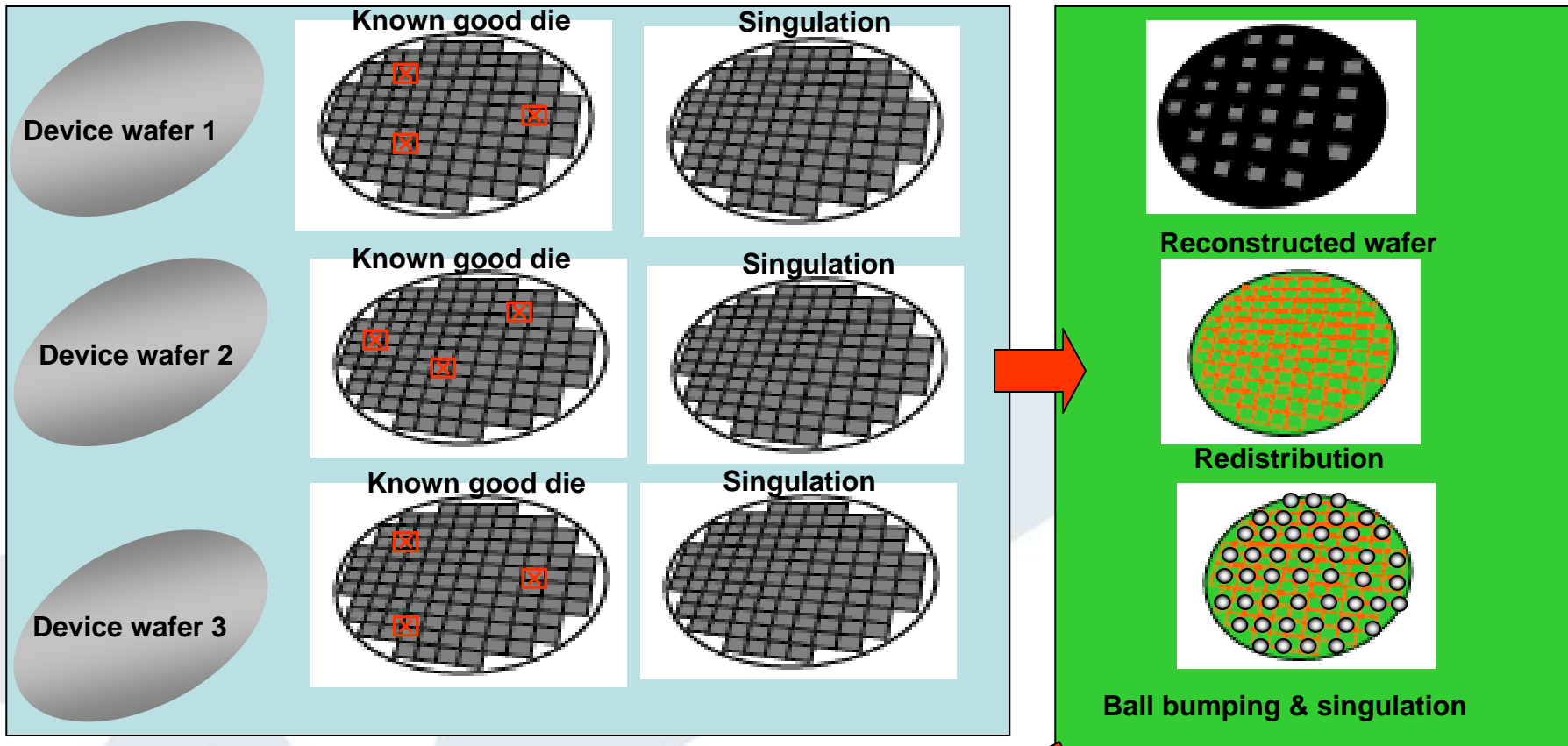
Embedded Micro Wafer Level Package (EM-WLP)

Proposed test vehicle

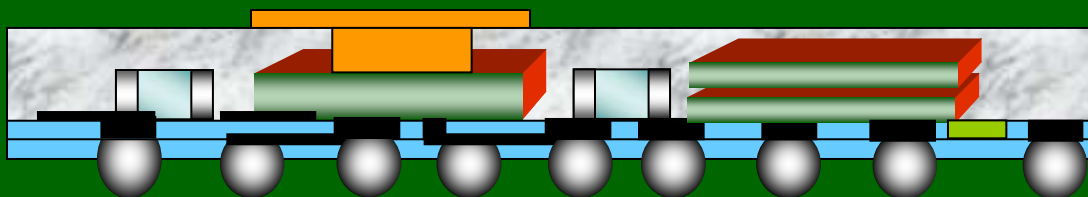


(Please note the package size and other dimension will be finalized based on members input)

Embedded Micro Wafer Level Package (EM-WLP) approach



Embedded Micro Wafer Level Package (EM-WLP)



Challenges with embedding Passives

- As the end product size shrinks, the cost of embedded passives goes down and the cost of using discrete passives goes up.
 - Smaller designs result in more embedded devices per panel
 - Smaller designs result in mechanical assembly challenges
- Performance comparison of amplifier

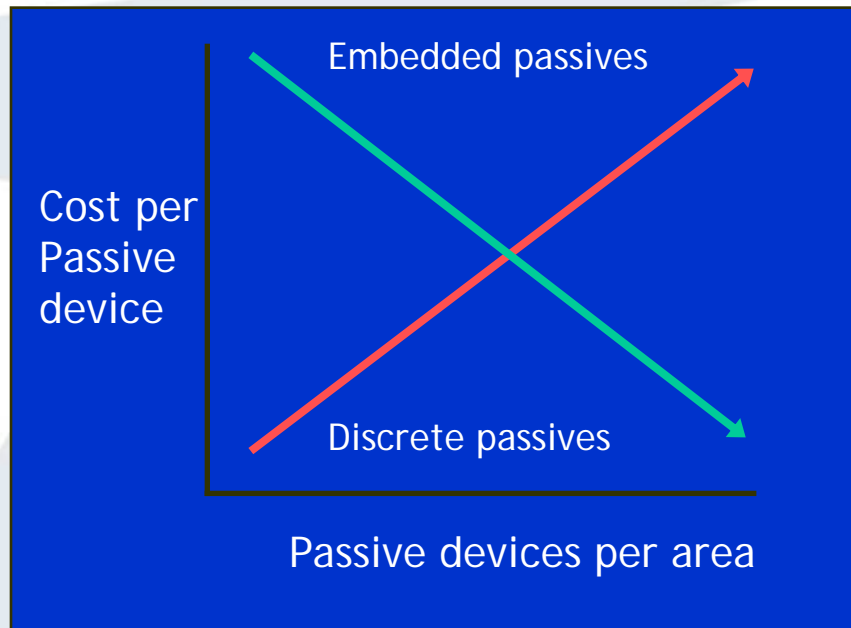
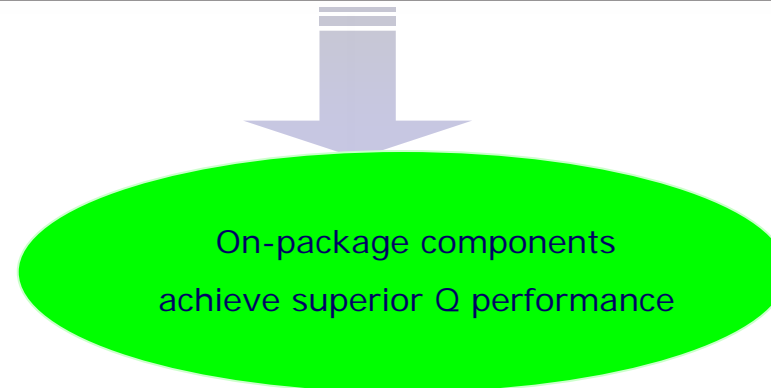


Table 2. Comparison of three different approaches of the power amplifier.

Passive integration	Pout (dBm)	Gain (dB)	PAE (%)	Area (mil × mil)
Fully on-package	26	17	48	900 × 500
On-chip interstage	23	15	32	511 × 472
Fully on-chip	19	10	20	105 × 84



(Source : IPC & Seoul Unniversity)

Challenges with Mold flow and Mold warpage

Table 1 : Comparison between Transfer Molding and Liquid Encapsulation

	Transfer Molding	Liquid Encapsulation
1. Thickness control	Excellent	Fair
2. Array warpage control	Good (low shrinkage compound)	Fair (glob top material)
3. Tooling cost	Medium	Low to none
4. Productivity (UPH)	High	Medium
5. Water adsorption (85%/85%RH/72 hrs)	0.3%	0.6%

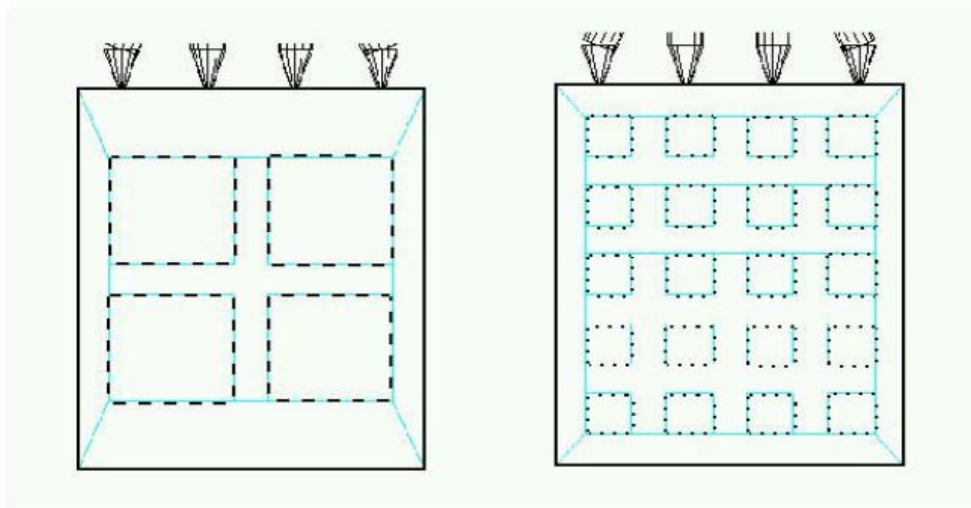


Figure 2 : Die Configurations for Mold Flow Simulation

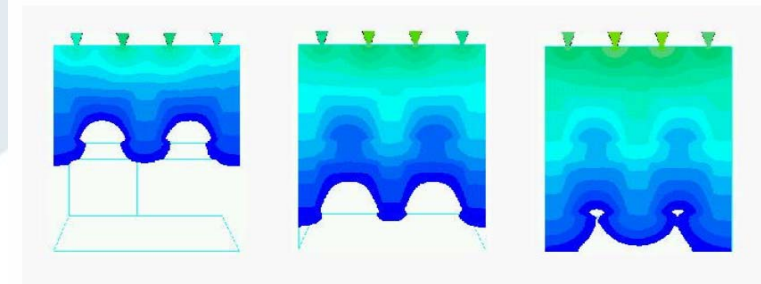


Figure 3 : Mold Flow Pattern for Thick Die Configuration (4 Up Array)

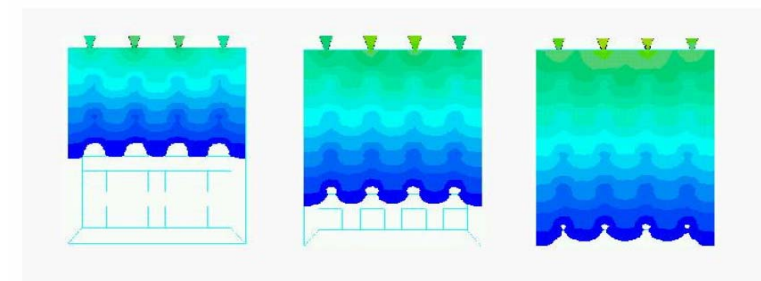


Figure 4 : Mold Flow Pattern for Thick Die Configuration (20 Up Array)

- Mold flow
- Thin profile
- Large area more warpage

(Source : ASAT)

Key Challenges

- **Wafer Level molding and warpage optimization**
- **Design guideline for RF, analog and digital integration**
- **Integration of multi-chip, chip passives and embedded passives**
- **Package embedded thermal enhancement structures**
- **Process methods for RDL and thin film passives on a molded substrate**
- **Materials for molding, adhesive tapes and DA**
- **Design guidelines for reconstructed wafer and RDL tolerances**
- **Wafer thinning**

Project Deliverables

A project report covering

- Thermo-mechanical analysis and structural optimization results of the package structure
- Signal and power integrity analysis and optimization
- Thermal optimization and enhancement results
- Wafer molding and warpage optimization results
- Material selection and characterization of EMC, adhesive tapes and die attach
- Fabrication details / flow of test vehicle with multilayer RDL for multi chip die integration
- Reliability assessment & Failure analysis of the package under Thermal cycle, MSL & Drop test