

S901: Two-Day Short Course on

“High-Performance Analog, RF, and mmWave CMOS Design”

When: Monday-Tuesday, 16-17 March 2009

Where: Institute of Microelectronics (IME), Singapore



Jointly Organized by
Exploit Technologies
(A member of A*STAR)
IEEE Singapore MTT/AP Chapter, and
IEEE Singapore Solid-State Circuits
Chapter



IEEE-RFIT Series Event

www.ieee-rfit.org



An Event NOT-TO-BE-MISSED!

This short course is targeting at both beginners and advanced RF/Analog IC designers.

The first day of this short course deals with the design of analog-to-digital converters (ADCs), phase-locked loops (PLLs), and low-voltage RF circuits, and the second day with millimeter-wave (mmWave) architectures and circuits. The emphasis is on design in deep submicron CMOS technology.

The first module analyzes two contenders for high-speed ADCs, namely, folding and interpolating architectures and pipelined architectures and presents examples of state of the art. The study culminates in 10-bit and 12-bit pipelined ADCs that calibrate gain error and nonlinearity and achieve record performance using op amps having a gain of less than 30.

The second module describes design issues and techniques for high-performance PLLs used in wireline and wireless applications. Various loop nonidealities, PLL architectures, and charge pump topologies are presented and low-noise, low-spur methods that allow a fast settling are discussed.

The third module addresses sub-1-volt RF design and describes techniques for low-noise amplifiers (LNAs), mixers, and oscillators. The problem of low-voltage broadband LNA design and the concept of noise-cancelling LNAs are presented and a number of downconversion and upconversion mixer topologies are examined.

Various properties of passive mixers are also described.

Our study of mmWave CMOS design on the second day begins with device modeling issues and techniques. A methodology for the modeling of inductors and transistors is presented that has been proven accurate up to 130 GHz in 90-nm CMOS technology. Next, architecture issues and the inextricable link between architecture design and circuit design are discussed. Circuit topologies for LNAs, mixers, and oscillators are then analyzed, and several examples of state-of-the-art transceivers are presented.

About the Instructor:



Behzad Razavi received the BSEE degree from Sharif University of Technology in 1985 and the MSEE and PhDEE degrees from Stanford University in 1988 and 1992, respectively. He was with AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. Since 1996, he has been Associate Professor and subsequently Professor of electrical engineering at University of California, Los Angeles. His current research includes wireless transceivers, frequency synthesizers, phase-locking and clock recovery for high-speed data communications, and data converters.

Professor Razavi was an Adjunct Professor at Princeton University from 1992 to 1994, and at Stanford University in 1995. He served on the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC) from 1993 to 2002 and VLSI Circuits Symposium from 1998 to 2002. He has also served as Guest Editor and Associate Editor of the *IEEE Journal of Solid-State Circuits*, *IEEE Transactions on Circuits and Systems*, and *International Journal of High Speed Electronics*.

Professor Razavi received the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the best paper award at the 1994 European Solid-State Circuits Conference, the best panel award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, and the best paper award at the IEEE Custom Integrated Circuits Conference in 1998. He was the co-recipient of both the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC. He received the Lockheed Martin Excellence in Teaching Award in 2006 and the UCLA Faculty Senate Teaching Award in 2007. He was also recognized as one of the top 10 authors in the 50-year history of ISSCC.

Professor Razavi is an IEEE Distinguished Lecturer, a Fellow of IEEE, and the author of *Principles of Data Conversion System Design* (IEEE Press, 1995), *RF Microelectronics* (Prentice Hall, 1998) (translated to Chinese, Japanese, and Korean), *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, 2001) (translated to Chinese and Japanese), *Design of Integrated Circuits for Optical Communications* (McGraw-Hill, 2003), and *Fundamentals of Microelectronics* (Wiley, 2006), and the editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (IEEE Press, 1996), and *Phase-Locking in High-Performance Systems* (IEEE Press, 2003).

Benefits of this Course

To learn directly from a world distinguished lecturer

- System driven considerations
- Building blocks challenges
- Device/process integration

Who Should Attend?

Engineers and technical staff, managers and business development personnel, students, who are keen on learning about RF and analog IC design in CMOS.

Date: Mon-Tue, 16-17 March 2009, Time: 0900 – 1700 (Registration starts at 8:30am)

Venue: Auditorium, [Institute of Microelectronics \(IME\), Singapore](#)
11 Science Park Road, Singapore Science Park II, Singapore 117685

Fees: **S\$990** for regular participant
S\$790 for IEEE Member by providing Membership No.
(discount for group registration from the same company: pay two get one free, pay five get three free)
S\$100 for regular students and
S\$75 for IEEE student members by providing Membership No.
(Hardcopy of lecture notes, Lunch and refreshments will be provided)
Registration Deadline: 10th March 2009

Registration Form

(IEEE Member #)

Name: _____ Email: _____

Name: _____ Email: _____

Name: _____ Email: _____

Company: _____

Address: _____

Tel: _____ Fax: _____

Email of contact person for group registration: _____

An invoice will be issued to your company upon successful registration.

Email to: Mary@atenga.sg, Short Course Administrator, Tel: +65 69030 9898 or Fax to: +65 6841 3986

Please email all technical enquiries to RFIT@ime.a-star.edu.sg,

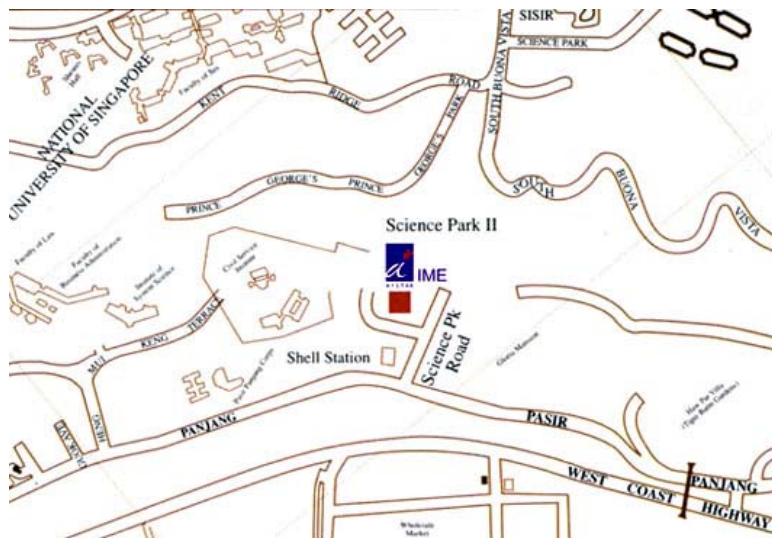
Other IME hosted events: http://www.ime.a-star.edu.sg/html/ev_events.html

Location Map

11 Science Park Road, Singapore Science Park II , Singapore 117685

Main line: (65) 6779 7522, Fax: (65) 6778 0136

The following buses serve Science Park II: Bus services 10, 30, 51, 143, **183**, 188, 200



Getting to IME

[1. Point to point driving directions from streetdirectory.com](#)

[2. SBS Transit Bus Guide](#)

[3. TIBS Bus Guide](#)