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Concerns and Future Prospects of 3D Integration Technology

GUEST SPEAKER

Prof. Lee Kangwook
Tohoku University
When: **5th August 2010, 4.00 p.m. to 5.00 p.m.**
Where: **Institute of Microelectronics, Singapore**
11 Science Park Road Singapore Science Park II Singapore 117685

Abstract

Three-dimensional (3D) integration and packaging is an emerging technology, which vertically stacks and interconnects multiple materials, technologies, and functional components such as processor, memory, sensors, logic, analog, and power ICs into one stacked chip to form highly integrated micro-nano systems. Since CMOS device scaling has stalled, 3D integration technology allows extending Moore`s law to ever high density, higher functionality and higher performance devices to be integrated with lower cost. The potential benefits of 3D integration can vary depending on approach; increased multi-functionality, increased performance, increased data bandwidth, reduced power, small form factor, reduced packaging volume, increased yield and reliability, flexible heterogeneous integration, and reduced overall costs. It is expected that the semiconductor industry`s paradigm will be shifted to a new industry-fusing technology era that will offer tremendous global opportunities for expanded use of 3D based technologies in highly integrated systems.

This talk will give an overview of 3D integration and packaging technologies, to discuss their benefits, applications, and to address key challenges associated with 3D technologies including motivations, key technology platforms, status, and perspectives toward commercialization. The challenges and concerns associated with reliabilities of electrical and mechanical constraints inducing by the wafer thinning, Cu TSV in a thinned device wafer including memory circuits for realizing high-reliable 3D circuits will be discussed.

Speaker Biography

Prof. Lee Kangwook (Member, IEEE) received the Ph.D. degrees in Machine Intelligence and Systems Engineering (currently Dept. of Bioengineering and Robotics) from Tohoku University, Sendai, Japan, in 2000. His Ph.D thesis was `Three Dimensional Integration Technology for Integrated Micro-Systems`. During the Ph.D course, he developed 3D Image Sensor (IEDM, 1999), 3D shared Memory (IEDM, 2000), and 3D Retina Chip (ISSCC, 2001) using wafer-level stacking technologies. From 2000 to 2001, he was a researcher for Japan Science and Technology Corporation, Sendai, Japan, where he was engaged in the development of wafer-level 3D integration technology for integrated micro-systems. From 2001 to 2002, he was a postdoctoral researcher at CIEEM, Electrical Engineering, Rensselaer Polytechnic Institute, Troy, New York, USA, where he joined the 3D processing technology research program funded by DARPA and developed the glue boning technology. From 2002 to 2008, he worked at Memory Division, Samsung Electronics Ltd. as a principal engineer, where he led the research and development of TSV based 3D stacking technology for high performance and high density electronic packaging/system. He also developed 2GB RS-MMC (2Gb NAND/8Chip, 2006), 4GB Lp DIMM (512Mb DDR2/4Chip, 2007) and 8GB Lp DIMM (1Gb DDR2/4Chip, 2008) prototype samples for the first time in the industry. He led the development of a new 3D DRAM (4Gb DDR3, 1Gb DDR3/4Chip, ISSCC 2009). He joined the Dept. of Bioengineering and Robotics, Tohoku University as a research associate professor in 2008. His current interests are three-dimensional (3D) stacked LSIs, 3D hybrid hetero-integrated opto-electronic systems, retinal prosthesis, and brain machine interface (BMI) implantable devices.

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Registration

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