

More Moore and More than Moore Meeting for 3D

GUEST SPEAKER

Dr. Simon Deleonibus
Chief Scientist
CEA-LETI

When: **11th February 2011, 10.30 a.m. to 11.30 a.m.**

Where: **Institute of Microelectronics, Singapore**
11 Science Park Road Singapore Science Park II Singapore 117685

Abstract

Nanoelectronics linear scaling appeals new 3D integration schemes in order to continue Moore's law. Unique opportunities exist to increase the devices performances, system complexity and reduce power consumption of mobile, handheld objects. New design and functional architectures will be possible by mixing logic and memory devices to save power consumption and introduce new applications by using neuromorphic or bio inspired approaches. Devices other than CMOS can be co-integrated with CMOS to interface the outside Multiphysics world (MEMS, sensors and actuators, RF devices, power devices,...) allowing new functionalities. 3D Wafer Level Packaging and System on a Wafer allow these new routes.

About the Speaker



Simon Deleonibus obtained his MSc and PhD in Applied Physics from Paris University, in 1979 and 1982 respectively. Since 2008, he is Chief Scientist (Directeur Scientifique) at LETI, watching at the Silicon Technologies Research (850 researchers).

He was with Thomson Semiconductors (Grenoble) in 1981 as a development and transfer to production process integration engineer. He joined LETI (CEA) in 1986 as a device engineering and process modules development expert for CMOS and Flash memories applications. From 1996 to 1999, he managed the Ultimate CMOS project. Subsequently, from 1999 to 2008, he was Director of the Electronic Nanodevices Laboratory (60 researchers), managing several Industrial, National and European funded projects.

He had published/submitted more than 550 conference and journal papers. He was the editor of 1 WSPC book, guest editor of 1 SSE special issue and authored 10 book chapters. He was also the editor of IEEE Transactions on Electron Devices and European Physical Journal - EPJ Applied Physics. He owns 30 patents: among them the initial patent on contact plug principle was widely used as a standard process by the semiconductor industry. Also, together with his team, he realized the first 20nm gate length MOSFET, world's smallest transistor in June 1999.

He was the program committee of several conferences, for instance; VLSI Technology Symposium, International Electron Devices Meeting (IEDM) and ESSDERC. He was also the member of the International Technology Roadmap of Semiconductors (ITRS), member of the Board of Directors of the Nanosciences Foundation and member of the European Research Council Engineering Panel. Since 1998, he lectures on microelectronics devices physics and technology and nanosciences at different Institutions and Universities, in France and Worldwide. He had also received several awards such as "Chevalier de l'Ordre National du Mérite" Decree of French Presidency and "2005 Grand Prix de l'Académie des Technologies - Prix Chéreau Lavet".

Registration

Pre-registration is required. Closing date is 9th February 2011. To register, please log on:
http://easstar.eventshub.sg/ems_wb_Details.aspx?CallID=28&EventID=157480

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