

# Design of Embedded Memory in Nano-scale CMOS Technology

## GUEST SPEAKER

**Prof. Kim Tae Hyung**  
Nanyang Technological University

When: **21<sup>st</sup> April 2011, 11.00 a.m. to 12.00 p.m.**  
Where: **Institute of Microelectronics, Singapore**  
11 Science Park Road Singapore Science Park II Singapore 117685

## **Abstract**

Transistor scaling has been the main driving force behind the semiconductor industry's growth. While billions of transistors can be implemented in a single chip, transistor scaling has generated a host of challenging issues. For circuit designers, increased power density and variability with scaling impose practical constraints on circuit designs. In order to keep Moore's Law valid and to continue leveraging semiconductor device technology, we must develop circuit techniques that address these problems.

Reliable memory design is one of the most challenging tasks in nano-scale CMOS technology due to the minimum or near-minimum sized devices and the high density requirement. This seminar presents various state-of-the-art circuit techniques for embedded memories (SRAM, eDRAM, Logic-compatible eDRAM, and Hybrid RAM), addressing major challenging issues such as variability, low power consumption, and ultra-low voltage operation.

## **About the Speaker**



Prof. Tony T. Kim received the B.S. and M.S. degrees in electrical engineering from Korea University, Seoul, Korea, in 1999 and 2001, respectively. He received the Ph.D. degree in electrical and computer engineering from University of Minnesota, Minneapolis, MN, USA in 2009. From 2001 to 2005, he worked for Samsung Electronics where he performed research on the design of high-speed SRAM memories, clock generators, and IO interface circuits. In 2007 ~ 2009 summer, he was with IBM T. J. Watson Research Center and Broadcom Corporation where he performed research on isolated NBTI/PBTI measurement circuits, SRAM Mismatch measurement test structures, and battery backed memory design, respectively. On November 2009, he joined Nanyang Technological University as an assistant professor.

He received AMD/CICC Student Scholarship Award in 2008, DAC/ISSCC Student Design Contest Award in 2008, Samsung Humantec Thesis Award in 2008, 2001, and 1999, and ETRI Journal Paper of the Year Award in 2005. He is an author/coauthor of 30+ journal and conference papers and has 7 US patents and 10 Korean patents registered. His current research interests include low power and high performance digital, mixed-mode, and memory circuit design, sub-threshold circuit design for high energy efficiency, variation and aging tolerant circuits and systems, and low power circuit techniques for 3D ICs.