

Novel Electronic and Optoelectronic Devices in Germanium Integrated on Silicon

GUEST SPEAKER

Prof Krishna C. Saraswat

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When: **6th July 2010, 3.00 p.m. to 4.00 p.m.**

Where: **Level 2 Auditorium, Institute of Microelectronics, Singapore**

11 Science Park Road Singapore Science Park II Singapore 117685

Abstract

Si CMOS technology has dominated the microelectronics industry, with continued scaling. However, future Si CMOS scaling is reaching practical and fundamental limits. To go beyond these limits on Si based devices, novel materials and structures are being aggressively studied. Ge shows much promise as an alternative to Si for both electronic and optical devices. In this talk, we will review recent results on heterogeneous integration of novel electronic and optoelectronic devices in Ge grown hetero-epitaxially on Si. In the recent, past Ge has shown much promise for high performance MOSFETs and optical detectors. More recently several other novel devices have emerged: tunnel FET (TFET), capacitorless quantum well single transistor DRAM (1T-QW DRAM), optical modulators and light emitters for on- and off-chip optical interconnects.

Speaker Biography



Krishna Saraswat received B.E. degree in Electronics from BITS, India, in 1968 and M.S. and Ph.D. degrees in Electrical Engineering from Stanford University in 1969 and 1974, respectively. He is Rickey/Nielsen Chair Professor in the School of Engineering, Professor of Electrical Engineering and Professor of Materials Science & Engineering (by courtesy) at Stanford University. During 1969-70, he worked on microwave transistors at Texas Instruments. He has been a technical advisor, board member and consultant to several industrial organizations in USA, Asia and Europe. He has also advised several academic and government organizations worldwide. Professor Saraswat's research interests are in new and innovative materials, structures, and process technology of silicon, germanium and III-V devices and interconnect for VLSI and nanoelectronics. Special areas of his interest are: new device structures to continue scaling MOS transistors, DRAMs and flash memories to nanometer regime, 3-dimensional ICs with multiple layers of heterogeneous devices, ultrathin MOS gate dielectrics, and metal and optical interconnections. He has graduated 70 doctoral students and has authored or co-authored over 600 technical papers, of which six have received *Best Paper Award*. He is a Fellow of the IEEE. He received the Thomas Callinan Award from The Electrochemical Society in 2000 for his contributions to the dielectric science and technology, the 2004 IEEE Andrew Grove Award for seminal contributions to silicon process technology, Inventor Recognition Award from MARCO/FCRP in 2007 and the Techno visionary Award from the India Semiconductor Association in 2007. He is listed by ISI as one of the 250 Highly Cited Authors in his field.

Registration

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