

Interconnect Design Issues in 3-D Integrated Systems

GUEST SPEAKER

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Swiss Federal Institute of Technology, Lausanne (EPFL)

When: **29th June 2011, 3.00 p.m. to 4.00 p.m.**

Where: **Institute of Microelectronics, Singapore**
11 Science Park Road Singapore Science Park II Singapore 117685

Abstract

The interconnect design process of vertically integrated systems demonstrates distinct differences as compared to the design of traditional planar integrated systems. The through-silicon-vias (TSVs), for example, constitute a new type of interconnect specific to 3-D ICs with considerably different electrical behavior as compared to conventional interconnects. In addition, the envisioned multilayer circuits face several design challenges. Among these challenges, signal and power integrity appear as predominant tasks that need to be resolved. This talk offers an overview of global interconnects issues, such as clock and power distribution in 3-D ICs. Specific approaches to distribute the clock signal within a 3-D IC are presented accompanied with experimental results. Related models for 3-D power distribution networks are also described. Furthermore, methods for efficient use of the TSVs for layer-to-layer signaling are presented. The role of the thermal issues in each of these interconnect design tasks is also discussed.

About the Speaker

Vasilis Pavlidis received the PhD degree from the Univ. of Rochester, Rochester NY, USA in 2008. Since September 2008, he is a postdoctoral researcher at the Integrated Systems Laboratory, EPFL with Prof. Giovanni De Micheli. His research interests are in the area of interconnect analysis and design, 3-D integration, networks on chip, and other issues related to VLSI design. He is the author of the book "Three-Dimensional Integrated Circuit Design," and the co-creator of the "Rochester cube," the fastest to date 3-D test circuit.

Registration

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